Phoenix
microsystems, inc.

Phoenix Instruction Book

5500

Data Communications Analyzer

Engineering New Standards in Technology

Phoenix microsystems, inc.
991 Discovery Drive
Huntsville, AL 35806

CONTROLLED DOCUMENT

September 1, 1986

To: Phoenix Model 5500 Data Communications Analyzer User

This revision to the first edition of the Model 5500 Instruction Book represents our sincere efforts to provide you, the user, with the most up-to-date and accurate instruction book possible. This revision incorporates change 1 and change two to the original edition as well as other changes to bring the instruction book current with existing software and hardware revisions. This instruction book contains the following sections:

1. Introduction - A brief overview of the 5500 and warranty information.

2. Description - The particulars of the 5500, physical, electrical, and environmental.

3. Installation - Safety summary, electrical connections, and packing and unpacking instructions.

4. Operation - The how-to's of basic 5500 operation.

5. Application - Specific instructions for particular testing.

6. Application Notes - Specific instructions, cookbook style, on specific testing.

7. Maintenance - How to keep your 5500 running in top condition.

8. Options - Instructions on the various options available with your 5500.

We would like your help. Send us a brief summary on how you use the model 5500 and we will convert it into an application note for inclusion in the manual. Send your ideas and suggestions to me at the address below.

Sincerely,

Dennis E. Crowley
Phoenix microsystems, inc.
991 Discovery Drive
Huntsville, AL 35806

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This instruction book includes:

Introduction

Description

Installation

Operation

Application

Application Notes

Maintenance

Options

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Caution

The material in this manual is subject to change. Before attempting any maintenance operation on the equipment covered in this manual, verify that you have a complete and up-to-date publication applicable to your equipment.

Please be advised that completion of the enclosed Warranty Registration Card and return to Phoenix Microsytems Inc., ensures you of manual revisions and service bulletin modifications to your equipment. Without the return of this card, Phoenix Microsystems Inc., bears no responsibility to forward this information to you.

Phoenix Microsystems has made every effort in making this manual concise, specific and error free. If yo find any errors or have any suggestions please notify us at the below address. We ask that you help use serve you, by describing your problem briefly and include the model number, paragraph or figure number and the page number.

Phoenix microsystems, inc.
991 Discovery Drive
Huntsville, AL 35806

Attn: Technical Writing Department

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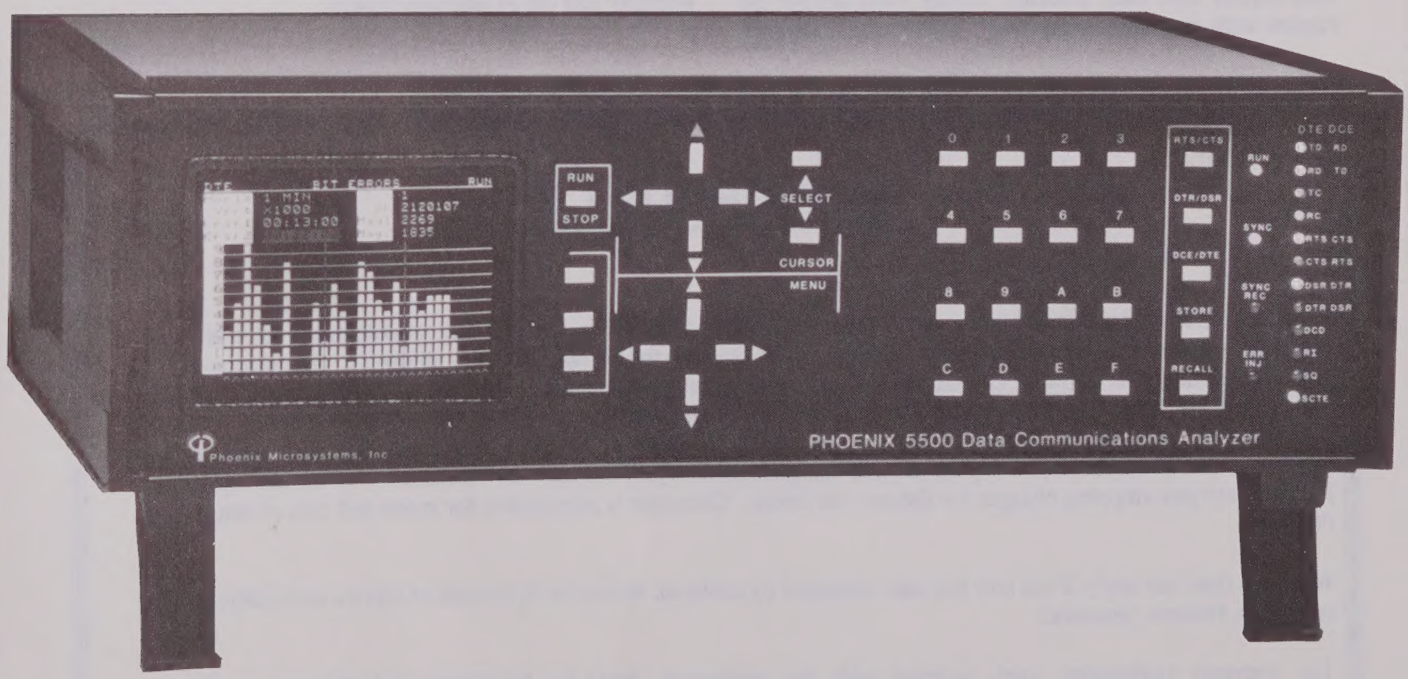
introduction

DESIGN FEATURES

The Model 5500 Data Communications Analyzer is the most powerful and versatile data error analyzer in its class. It will measure up to 23 error performance parameters, plus frequency, bias distortion, event time, and (optional) phase shift jitter simultaneously. Among the features of the 5500 are:

- ° Software control to keep current with changing technology.
- ° RS-232 and IEEE-488 remote control ports.
- ° Covers 50 bps to 13 Mbps including the DS1 and DS1C rates.
- ° All plug-in interface modules have full DCE/DTE capability.
- ° Selectable bit error and bipolar violation injection caability.
- ° Graphic display of error parameters versus time for up to 60 hours in one minute intervals.
- ° Hard copy printout of test reults with optional printer.
- ° Video out (RS-170) for remote monitor.



Phoenix Model 5500 Data Communications Analyzer

INSTRUCTION BOOK

The 5500 Data Communications Analyzer instruction book includes all the instructions on the basic unit and supports operation of the basic unit. Included also are any supplements necessary to define and support different configurations of the 5500. Also included are the instructions for the various options available with the 5500. The instruction book represents the latest software and hardware configuration available at the time of printing. Changes to maintain the instruction book will be published as required.

CUSTOMER SERVICE

For warranty work or questions about the 5500 contact:

Customer Service Manager
Phoenix microsystems, inc.
8290 Whitesburg Drive
Huntsville, Alabama 35802

Telephone: 1-800 826 6798 USA
1-205 881 2173 USA
Telex # 752592 (PMIHTV)

PASS PROGRAM

An extended Product Assurance Support Service (PASS) program is available to meet the needs of those customers who require that their Phoenix Model 5500 always be current with the latest technology. While our customer service department will always answer questions regarding a malfunction in your 5500, we offer extended support for customers who desire to keep abreast of the latest in product design and want the expertise of Phoenix factory service to meet their repair needs.

While your 5500 is enrolled in the PASS program you will receive: free software enhancements for all new standard features added to the 5500; no labor charge for installation of new hardware updates to the Model 5500; no-charge repairs for your 5500; free use of a 5500 during the repair of your 5500 (if requested); remote diagnostic assistance via modem link (must be scheduled in advance); annual no charge performance/calibration verification of your 5500; instruction book updates; hardware and software updates to correct 'bugs' that may develop; and software updates that provide easier operation of the existing features on your 5500.

In addition you will receive a password to allow you to access the Phoenix Bulletin Board. This electronic bulletin board will have a trouble message center, software enhancement announcements, application notes, and new product announcements.

To enroll your Phoenix 5500 in the PASS program, contact Phoenix Customer Service at the address/number below. The PASS program is available for both in-warranty and out of warranty 5500's.

WARRANTY

Phoenix microsystems, inc. warrants each Model 5500 against defects in material and workmanship for a period of one year (options are also warranted for one year) from the date the Model 5500 was shipped to the customer. If at any time during the warranty period, the Model 5500 should malfunction, Phoenix will repair, or at Phoenix's option, replace the unit free of charge. The remedies listed herein are the users sole and exclusive remedies. Phoenix microsystems, inc. shall not be liable for any indirect, direct, incidental, or consequential damages. Owner must return the unit to the factory, shipping prepaid and packaged to best commercial standard for electronic equipment. Phoenix will pay shipping charges for delivery on return. Customer is responsible for mode and cost of shipment to Phoenix.

Warranty does not apply if the unit has been damaged by accident, misuse or as a result of service or modification by other than Phoenix personnel.

The warranty registration card, shipped with the equipment, must be completed and returned to Phoenix microsystems, inc. to validate this warranty.

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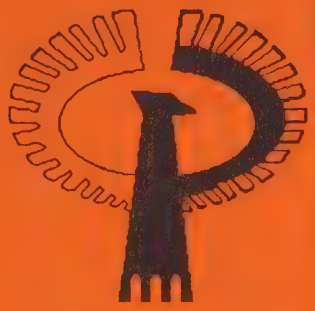

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description

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description

1.1 GENERAL

The Model 5500 Data Communications Analyzer is the most comprehensive and advanced error rate and PHASE jitter test set presently available. The 5500 provides error performance measurements on a wide variety of communications systems from 75 bps to 13 Mbps. Over 23 different performance parameters may be measured simultaneously, along with received clock frequency measurements, control signal event time, optional low frequency edge jitter (to 72 kbps), and T-1 phase jitter measurement (spectrum analysis and wideband) and generation test capability. All key test parameters may be printed upon user selected conditions, or graphed in a TIME vs AMPLITUDE 60 hour display for long term testing.

The 5500 accepts modular interfaces for all USA, European, and Pacific Rim standard data and TELCO communications links.

All test capabilities can be fully REMOTED via IEEE-488 or RS-232 control. The 5500 is the instrument to provide testing at unmanned sites.

Key features of the Phoenix Model 5500 include:

- Measurement of 23 Simultaneous BERT Test Parameters
- Histogram Graph of any Test Parameter for up to 60 hours
- Frequency Measurements of Received Clock to 16 MHz
- Bias Distortion Measurement
- Modular Interfaces for virtually all communications links
- Event Time measurement of Interface Control Signal to 1 us
- Test Patterns
  All standard pseudorandom patterns
  T-1 Set and Reset code generation
  Memory buffer to allow user to enter own patterns
- Optional low frequency edge jitter (to 72 kbps)
- Optional T-1 and G.702-2048 phase jitter
  Complete spectrum analysis
  Wide band measurement
  Peak long term jitter storage
  AT&T or CCITT built-in mask display
  Sine, triangle, or "Mask" jitter generation sweep
  Full printout capability
- Optional G.821 "ISDN" data collection software package
- Complete remote control via RS-232 or IEEE-488 control bus

1.2 EQUIPMENT SUPPLIED

The 5500 is supplied with the following:

1. Instruction Book
2. Power Cord
3. Model 5500-200 RS-232 Interface Module

1.3 OPTIONS

Table 1-1 presents the Interface options available for the Model 5500 while table 1-2 presents remaining, non-interface options.

Table 1-1. Interface Options

MODEL	FUNCTION
5500-200	RS-232 DCE/DTE/MIL STD 188C
5500-275	5500-200 with 604 compatible framing option
5500-300	CCITT V.35 DCE/DTE Module
5500-375	5500-300 with 604 compatible framing option
5500-400	RS-449 (RS-422 & RS-423) DCE/DT Module
5500-450	RS-449/MIL-STD 188/MIL-STD 188-100
5500-475	5500-400 with 604 compatible framing pattern
5500-500	TTL Module
5500-538	DDS Interface
5500-555	I/O control module to interface 5500 with 5500-MSU
5500-600	DS-1/DS1C Unframed Module
5500-624	DS-1 Framed/Unframed Module
5500-700	DS-2 Unframed Module
5500-800	CCITT G.703 (2.048 Mbps) Module
5500-805	CCITT G.703 (8.448 Mbps) Module
5500-810	CCITT G.703 (64 Kbps) Module
5500-815	Same as 5500-800 with J05 option
5500-900	Bell 303 Module

Table 1-2. Options

MODEL	FUNCTION
5500-J01	Jitter measurement below 72 Kbps
5500-J02	Jitter measurement and injection at T1
5500-J05	Jitter measurement at G.703 (2.048 MHz)
5500-CL01	Precision clock option (+/- 1PPM accuracy for all internal rates below 1 Mhz)
5500-CL02	Precision clock for one frequency (75 Hz to 13 MHz)
5500-PO1	Printer with graphics capability
5500-DM01	12" CRT display monitor
5500-RK19	19" rack mount kit
5500-ECCP	Industrial grade aluminum carrying case
5500-ECCV	Padded vinyl carrying case
5500-232	5 foot RS-232 25 conductor cable*
5500-488	5 foot IEEE-488 24 conductor cable*
5500-488E	Same as 5500-488 with additional connector for parallel connection of multiple units on control bus.
	*specify male-to-male, female-to-female, or female-to-male

1.4 EQUIPMENT SPECIFICATIONS

Table 1-3 presents the 5500 equipment specifications.

Table 1-3. Equipment Specifications

CHARACTERISTIC	SPECIFICATION
Electrical	
Input	
Voltage	Selectable 110/220 VAC +/- 10%
Frequency	50/60 Hz
Power	100 Volt-amperes maximum
Video Output	RS-170 Composite
Frequency Counter	
Range	75 Hz to 16 MHz
Accuracy	+/- .0005% standard +/- LSD
External Clock Input	
Range	50 Hz to 13 MHz
Logic	"1" = 5+/-.05 volts VDC "0" = 0+/- .4VDC
Load	10 TTL loads
Environmental	
Temperature	
Operating	0 to 50 degrees C
Storage	-10 to 85 degrees C
Physical	
Dimensions	
Length	12.79 inches
Width	17.20 inches
Depth	5.25 inches
Weight	23 pounds

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Data Communications
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installation

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2.1 GENERAL

This section contains information necessary for the correct installation of the Phoenix Model 5500 Data Communications Analyzer. Included are initial inspection procedures, power and grounding requirements, and procedures for repackaging the instrument for shipment.

2.2 UNPACKING AND INSPECTION

The 5500 is carefully packaged to prevent damage in shipment. Upon receipt carefully inspect the condition of the shipping container and retain it for future use. After unpacking, examine the exterior of the unit to insure it is free of scratches, dents, and any other visible signs of damage.

If the 5500 was damaged in shipment, file a claim with the carrier immediately. Check to insure you have received the supplied accessories (listed in paragraph 1-2 of this manual).

2.3 SAFETY SUMMARY

The following safety precautions must be observed whenever the 5500 is operated, serviced, or repaired. Failure to comply with these and other specific warnings within this manual is a violation of Phoenix Microsystems' safety standards of design, manufacture, and intended use of the test set. Phoenix Microsystems assumes no liability for the customer's or user's failure to comply with these precautions.

GROUNDING

The 5500 chassis and cabinet must be connected to an electrical ground for proper operation and to minimize shock hazard. The unit is furnished with a three conductor AC power cable which incorporates a ground lead. The power cable must be connected to an approved three-contact electrical outlet or to a three conductor to two conductor adapter with a grounding wire (green) connected to electrical ground at the outlet.

EXPLOSIVE ATMOSPHERE

The 5500 must never be operated in the presence of any flammable gases or fumes. Power must not be applied to this or any instrument under such conditions due to the potential for explosion.

HIGH VOLTAGE CIRCUITS

Only qualified maintenance personnel should remove the instruments covers. Dangerous voltages may exist within the unit even after the power cable has been disconnected. Do not attempt to replace components with the power cable connected. To avoid possible serious injury always disconnect the power and discharge circuits, particularly near the CRT, before touching any internal circuits or components.

SERVICE AND ADJUSTMENT

The 5500 contains few user serviceable parts. Internal servaice or adjustment should only be performed by Phoenix Microsystems' repair personnel or authorized maintenance facilities to ensure that the safety features of the instrument are not compromised.

CATHODE RAY TUBE (CRT)

Use caution when handling the CRT. To avoid breakage of the CRT and the resulting implosion do not jar or handle the 5500 in a rough manner while the internal circuitry is exposed. Removal, repair, or replacement of the CRT should only be done by qualified maintenance personnel.

LINE VOLTAGE

Before connecting the AC power cord make sure that the line voltage switch on the 5500 power supply module is set to match the source voltage.

FUSES

Always replace a blown fuse with an identical replacement fuse. Never use a fuse of a larger value or attempt to defeat or bypass the fuse.

ENVIROMENTAL

Do not exceed the operating temperature limits (0 to 50 degrees C).

INTERFACE MODULES

Do not apply power to the 5500 without an interface module plugged into the unit. **Never** remove or insert an interface module into the 5500 with the power on. Always remove power first or damage to the module and/or the 5500 may result.

2.4 PRE INSTALLATION CHECK

The 5500 may be operated from any power source supplying 100 to 120 volts AC, or 220 to 240 volts AC, 47 to 66 Hz, single phase AC.

WARNING

Damage to the unit may result if the line voltage is not selected to match the input power source

The 5500 is shipped from the factory preset for operation from a 110 VAC, 60Hz source. To operate the unit from a 220 VAC source, the following steps must be followed:

1. Locate the 5500 power supply module on the rear of the 5500 (refer to figure 2-1).

2. Remove and retain the four Phillips head screws that hold the power supply module to the 5500.

3. Slide the power supply module out of the 5500.

4. Locate the 110 VAC/220 VAC red slide switch. (refer to figure 2-2)

5. Place the 110 VAC/220 VAC switch in the 220 VAC position.

6. Install a 1 amp, fast blow fuse in the line fuse holder on the rear of the power supply module.

7. Slide the power supply module back into the 5500.

8. Replace the four screws removed in step 2.

The 5500 is now ready for operation at 220-240 VAC.

2.4.1 50/60 Hertz Selection

Upon initialization, the Model 5500 video frequency defaults to 60 hertz. User may select either 50 or 60 hertz by pressing the 6 (for 60 hz) or 5 (for 50 hz) on the key pad upon power up. This key must be the first key pressed after power up. After the key is pressed, the value is stored in non volatile RAM and all future power ups will come up at the last chosen frequency.

2.4.2 5500 CRT Saver

Upon initialization the 5500 defaults to CRT saver OFF. The user may enable the CRT saver by pressing a 2 on the keypad as the first key pressed upon power up. (Pressing a 3 disables CRT saver.) When the CRT saver is enabled, the video screen will be disabled 20 minutes after the last key has been depressed. Pressing any key will re-enable the video for another 20 minutes. The CRT saver enable/disable is stored in non volatile RAM and remains at its last setting until changed.

2.5 REMOTE/PRINTER PORT CONFIGURATION

The 5500 RS232 remote port is capable of connecting to either a DCE type device or a DTE. There are 6 selector (3 sets of 2) switches on the 5500 control board that must be configured for the device connected to the port.

To gain access to these switches, the top cover on the 5500 must be removed. This is accomplished by removing two screws holding the top rear retaining bezel, and then sliding the top cover and bezel back.

The three sets of switches are mounted on the main PC near the RS232 port connector. Each switch has DCE, DTE indications screened on the PC. If a terminal type device, such as a CRT or printer is connected to the RS232 port, set all switches to the DCE position. If a DCE type device, such as a modem is connected, set all switches to DTE position.

Table 2-1 lists the interface signals and their function for DCE and DTE with the corresponding pin assignments.

2.6 PACKAGING FOR SHIPMENT

Use the original packing material, if available, when packing the 5500 for shipment. If the original material is not available, package the 5500 to the current best commerical standards for electronic equipment. Phoenix Microsystems' customer service department can provide information and recommendations on packing materials to be used.

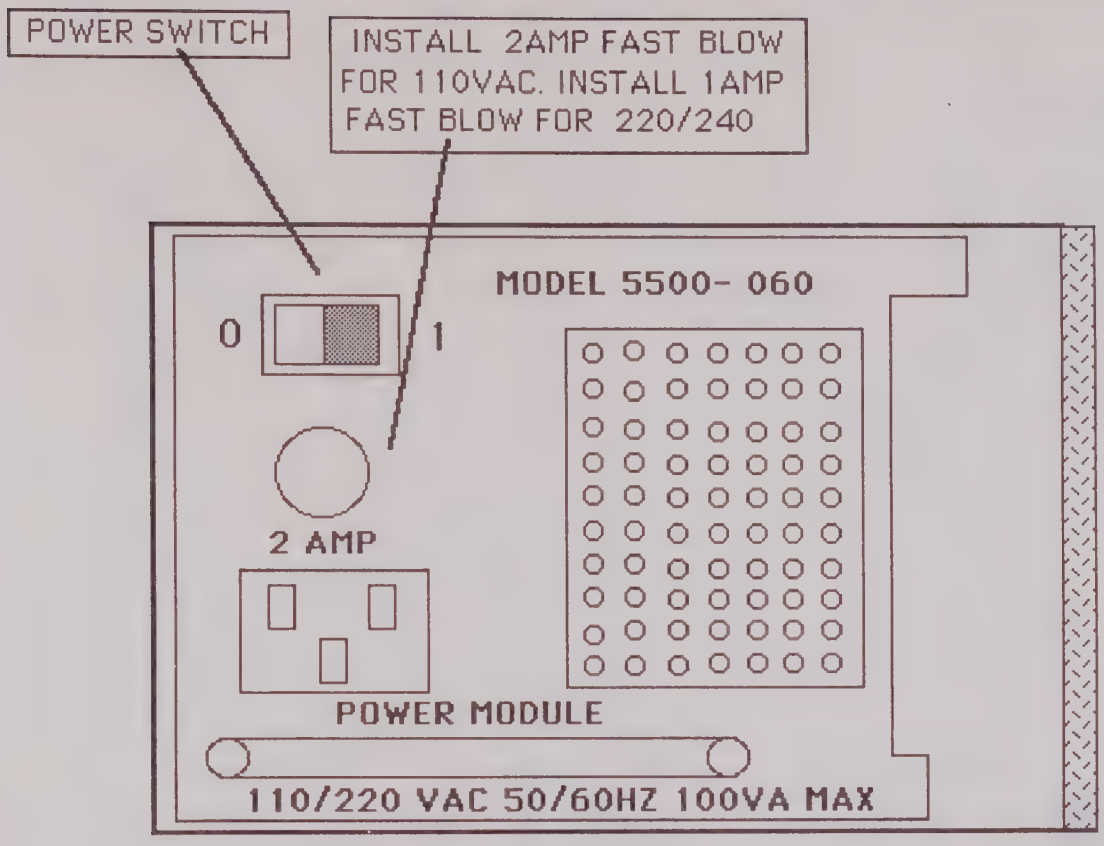

Figure 2-1. 5500 Power Supply Module

Table 2-1. Remote Port Pin Assignments

PIN	FUNCTION		SOURCE	
	DTE	DCE	DTE	DCE
2	TXD	TXD	5500	USER
3	RXD	RXD	USER	5500
4	RTS	RTS	5500	USER
5	CTS	CTS	USER	5500
6	DSR	DSR	USER	5500
7	Signal Ground	Signal Ground	-----	-----
8	DCD	DTR	USER	USER
20	DTR	-----	5500	-----

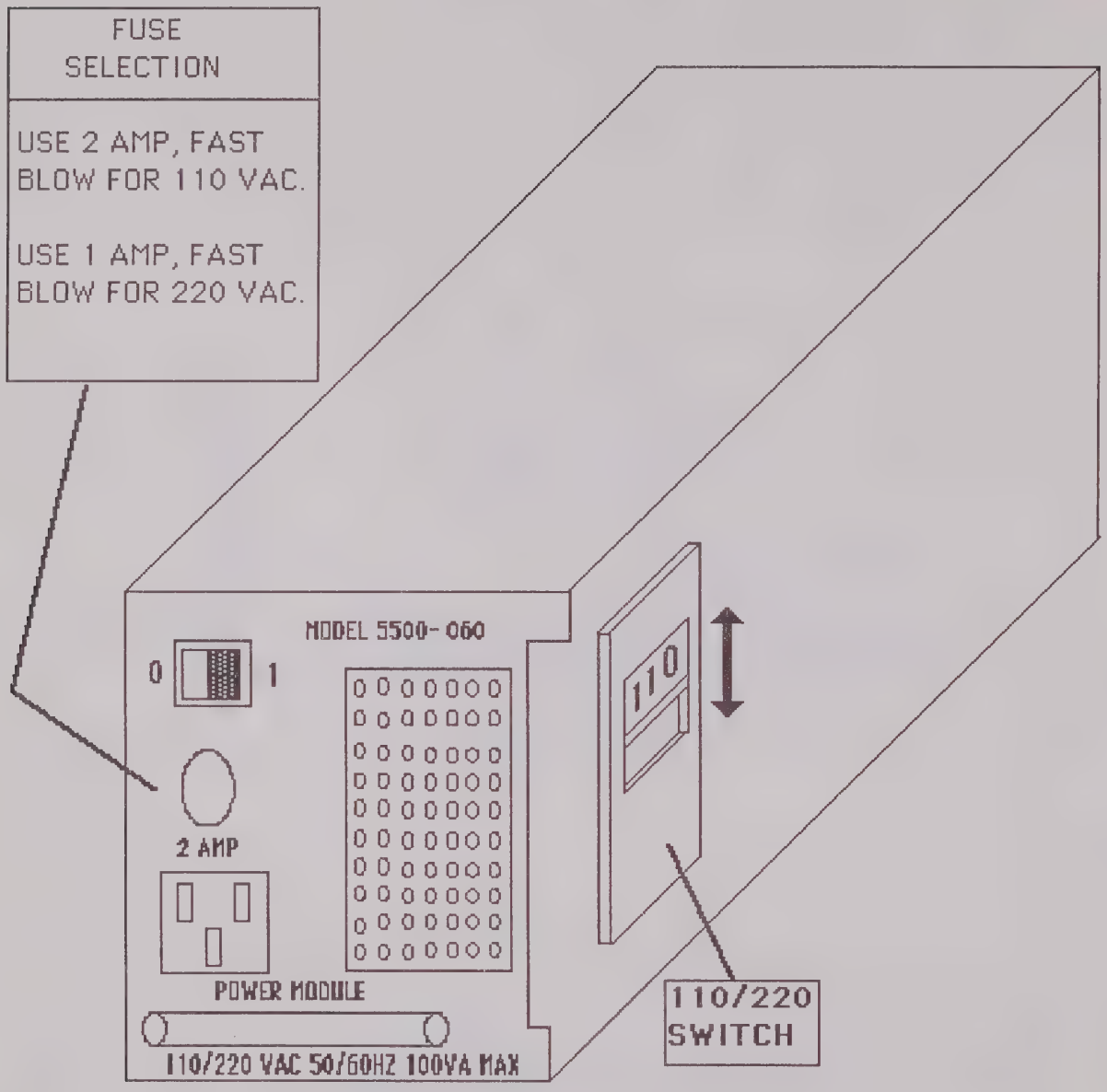

Figure 2-2. 110/220 Switch Location

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3.1 GENERAL

The Phoenix Model 5500 Data Communications Analyzer is a versatile, powerful test instrument designed to be flexible enough to prevent rapid obsolescence while retaining an easy operator interface. The model 5500 accomplishes this task by using Menu driven software and allowing the operator to store up to ten complete test programs. The Model 5500 then enables the user to have "one-button" testing by recalling stored programs. At the same time the user is free to change any of the test conditions or parameters providing the utmost in testing flexibility.

The following paragraphs outline the setup procedures for all aspects of Bit Error and Jitter testing using the Model 5500. The procedures are presented using graphic representations of the Model 5500 front panel controls, menus, and test displays. All parameter and test setup selections are detailed for each display menu.

3.2 CONTROLS AND INDICATORS

Table 3-1 presents the controls and indicators for the Model 5500 Data Communications Analyzer. Figure 3-1 is a multi-page drawing of the controls and indicators and it is keyed numerically to table 3-1.

Table 3.1. Controls and Indicators.

INDEX NO	CONTROL OR INDICATOR	FUNCTION
1	RUN STOP	Controls test set operation. RUN led will be on when in RUN mode.
2	CURSOR keys.	Select the desired item to be changed on menu. A half intensity cusor appears around selected item.
3	SELECT	Activates the selected parameter for each test option.
4	MENU	Selects menu to be displayed. (Refer to figure 2.4 for menu map.)
5,6,7	Soft keys	Control the function displayed on display opposite key.

Table 3.1. Controls and Indicators. (cont.)

INDEX NO	CONTROL OR INDICATOR	FUNCTION
8	Hex keys	Hexidecimal keypad used for data entry.
9	DCE/DTE	Selects DCE or DTE mode on interface module.
10	DTR/DSR	Toggles DTR in the DTE mode and DSR in the DCE mode.
11	RTS/DCD	Toggles RTS in DTE mode and DCD in DCE mode.
12	SYNC	Indicates that the 5500 is in sync with incoming data.
13	RUN	Indicates run mode selected.
14	DTE DCE	Interface activity indicators.
15	ERR INJ	Indicates errors are being injected in the output data.
16	SYNC REC	Indicates 5500 has recovered sync after losing sync due to errors in incoming data.
17	RECALL	Dual function key. Press once to obtain Menu Matrix Help menu and press twice to recall pre-programed test.
18	STORE	Stores current test in selected memory for recall. (0 to 9)
19	5 and 6 keys	50/60 Hz selection. Hold down 5 for 50Hz or 6 for 60Hz during power up. (Defaults to last setting if neither 5 or 6 selected.)
20	Power Switch	Controls main power to 5500.

Table 3.1. Controls and Indicators.(Cont.)

INDEX NO	CONTROL OR INDICATOR	FUNCTION
21	Line Fuse	2 amp fast blow fuse for 110 VAC operation. 1 amp fast blow for 220 VAC operation.
22	Test Points	Test points to which an oscilliscope may be connected. Test points are defined as follows: TXD: 5500 transmit data RXD: Received data TXC: Transmit clock RC: Receive clock XMIT PAT: Transmit pattern sync REC PAT: Receive pattern sync ERR: BIT error sync REC SYNC: 5500 in sync SP: Spare GND: Ground
23	RS-232	RS-232 remote port connector
24	IEEE-488	IEEE-488 remote port connector
25	BRIGHTNESS	5500 CRT brightness adjustment
26	VIDEO	RS-170 composite video output
27	USER CLK	Connector to input a clock. When selected, entire 5500 operation is slaved to this clock
28	Interface port	Port to which inter-face modules are

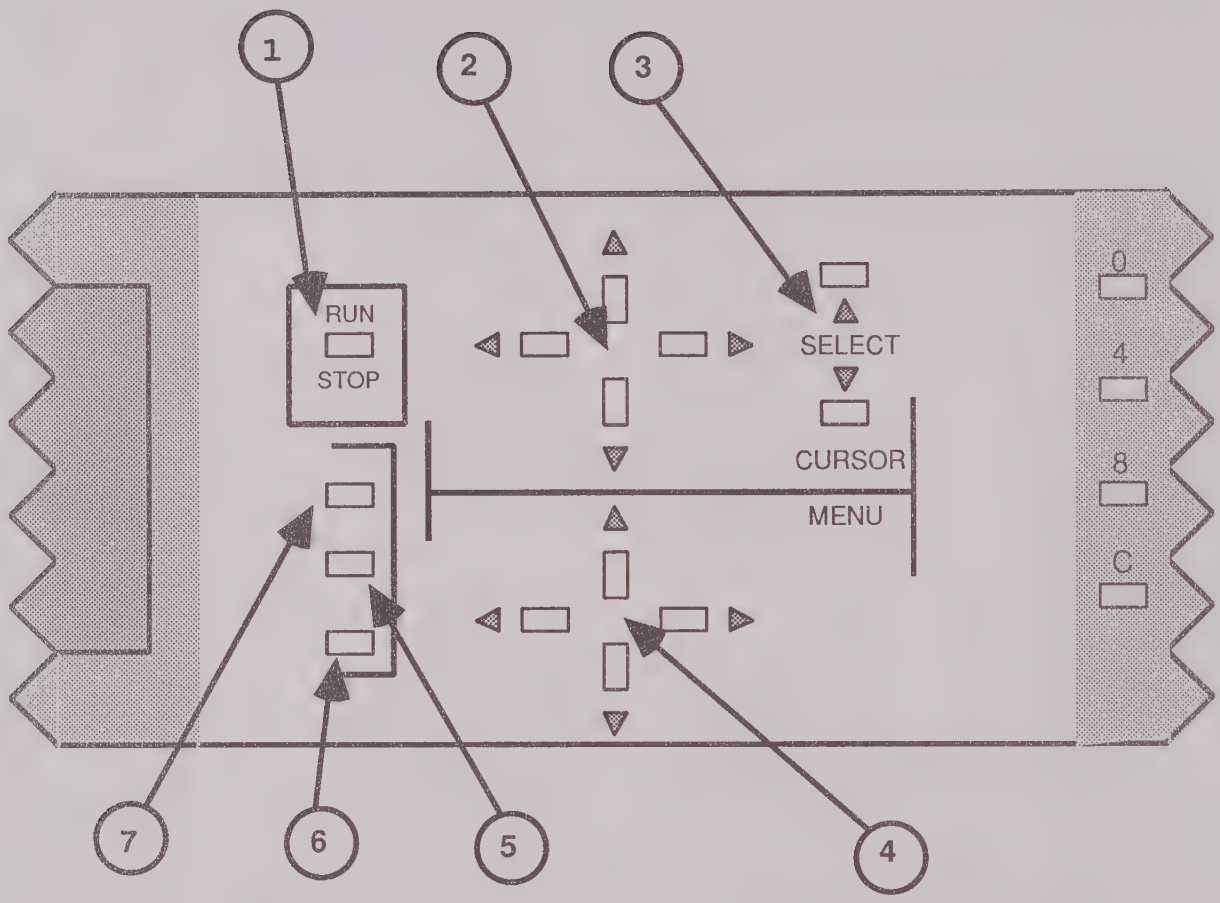


Figure 3-1. Controls and Indicators.
Sheet 1

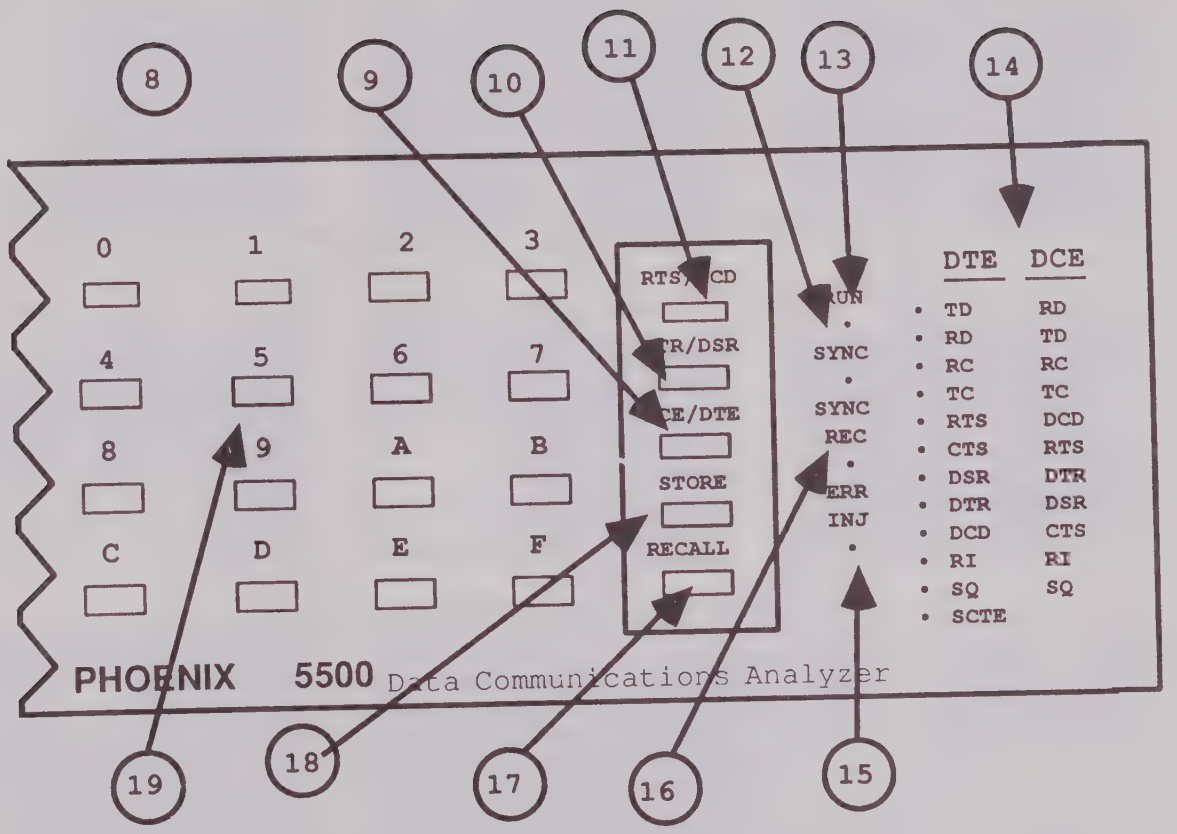
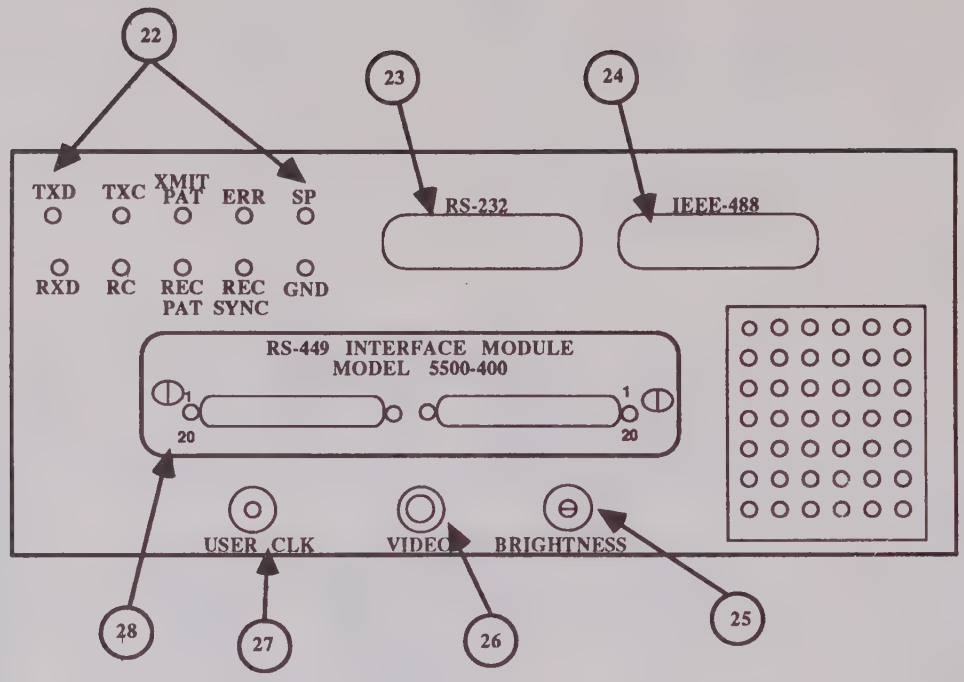


Figure 3-1. Controls and Indicators
Sheet 2



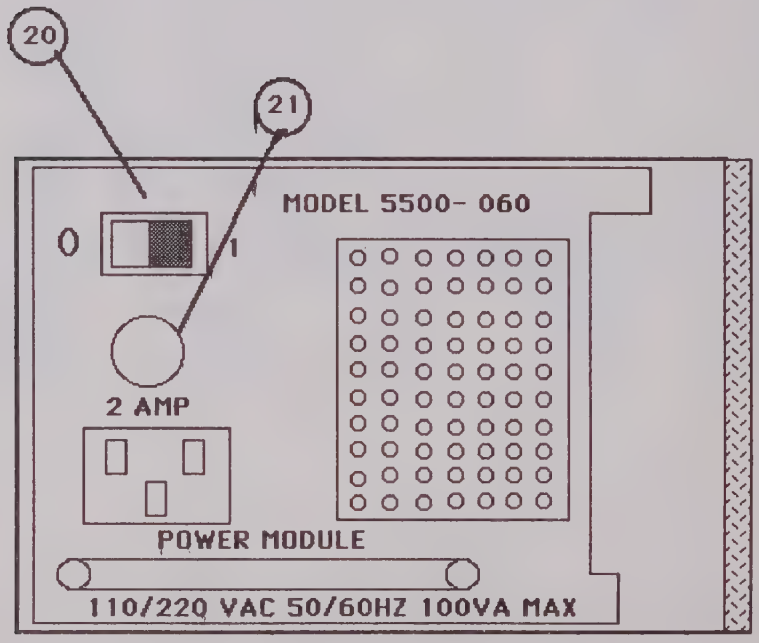
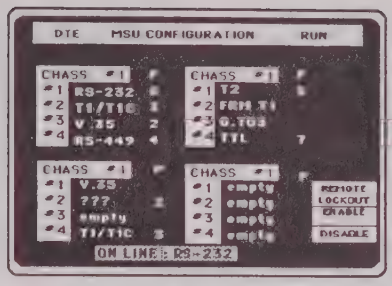


Figure 3-1. Controls and Indicators
Sheet 3



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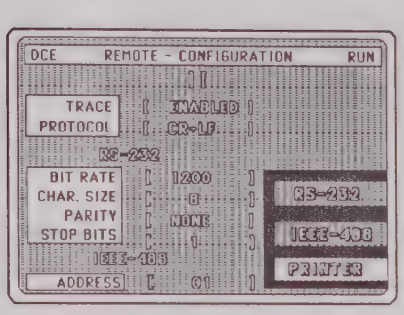
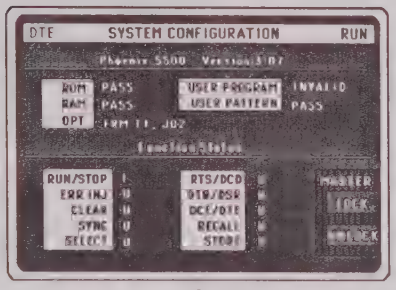
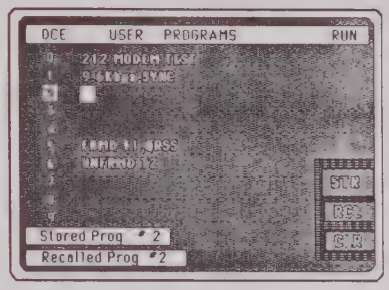
*** These menus only present if option for that menu is installed**



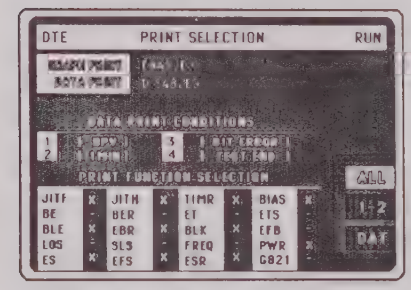
2



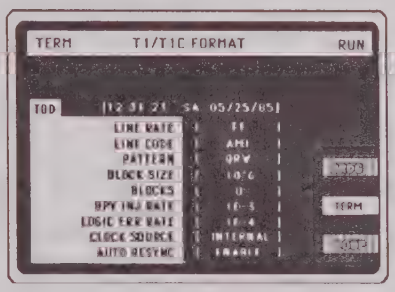
3



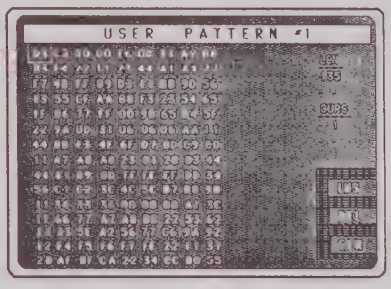
4



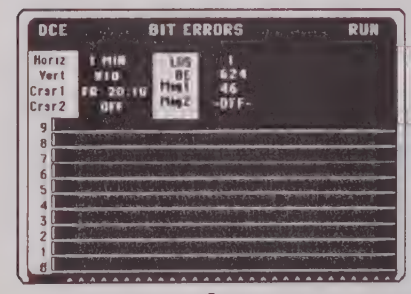
5



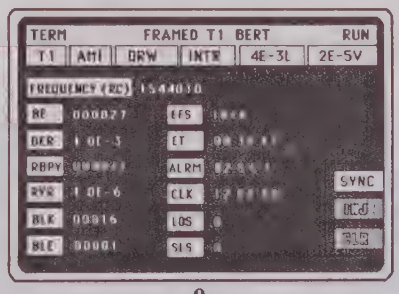
6



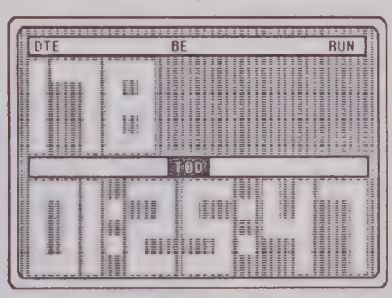
7



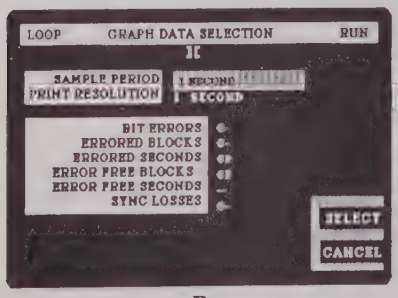
8



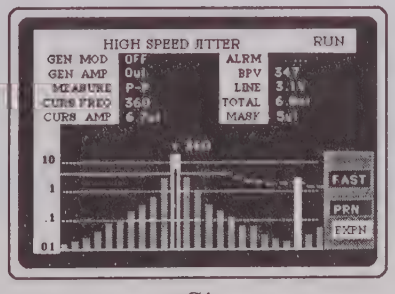
9



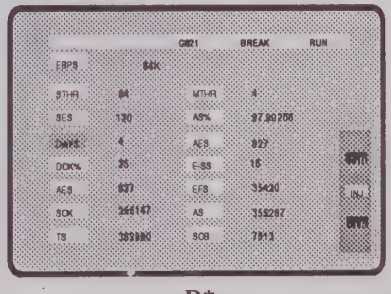
A



B



C*



D*

Figure 3-2. Menu Matrix Location

3.3 INITIAL SET UP PROCEDURES

The purpose of this section is to provide to the operator elementry instruction for using the basic functions of the Model 5500. It is not intended to provide in-depth coverage of each function. It is a straightforward, step by step, illustrated procedure for setting up, operating, and obtaining test results for some of the more basic Bit Error tests.

3.3.1 Turn-on

1. With power removed, plug in the desired interface module into the rear panel slot and fasten with the two retaining screws.

2. Connect cables from either the DCE or DTE connector on the module to the device under test. It makes no difference to the Model 5500 which connector is used; the choice is the operators option depending upon the cable connector.

3. Connect the Model 5500 to AC power. Normal operation requires 110 VAC, 60Hz. Refer to section 2.3 of this manual for operation at 230 VAC, 50Hz.

4. Turn Power Switch (located on rear panel) to ON.

5. The matrix of menus is shown in figure 3.2 and provides a map which allows the user to locate the desired display. Depressing the **RECALL** switch one time will bring the MATRIX HELP MENU to the screen.

3.3.2 BERT Display

1. When power is initially applied to the Model 5500 BLACK BERT will appear followed by BERT Display as shown in figure 3-4 or the SYSTEM CONFIGURATION menu as shown in figure 3-5.

2. Depress the RECALL switch one time to bring the MENU MATRIX HELP menu (figure 3-3) to the screen.

3. When in the MENU MATRIX HELP display, a particuliar menu may be selected by either of two methods.

a. The cursor SELECT key may be used to move the cursor over the desired menu name or matrix number and then press the GO TO softkey.

b. The number of the selected menu may be entered from the front panel key pad and then press the GO TO softkey.

4. The unit enters a self test when power is applied and if it is not operating correctly the SYSTEM CONFIGURATION menu will be displayed as shown in figure 3.5 instead of MAIN BERT DISPLAY. Refer to step 16.

5. The basic test set up parameters are located at the top of the MAIN BERT DISPLAY and may be changed while tests are being run if desired.

6. Configure the set as terminal (DTE) or modem (DCE) as appropriate for the device under test using the front panel toggle key labeled DCE/DTE. The upper left hand corner of the CRT display shows the state of the Model 5500. To test a modem, set the Model 5500 to act as terminal (DTE) and vice versa.

7. Using the UP MENU cursor key, change to the BERT FORMAT menu located directly above the MAIN BERT DISPLAY.

8. Use the CURSOR key to highlight the parameters to be changed if any. Once the half intensity block has been moved over the desired parameter the user can scroll through the different choices for that parameter using either the UP or DOWN SELECT key.

9. Once the operator has become familiar with the parameter choices it is not really necessary to use the BERT FORMAT menu in most cases. The important test parameters can be changed on the MAIN BERT DISPLAY by using the CURSOR keys to highlight the parameter at the top of the CRT display and then using the SELECT keys to change them.

10. Change the highlighted parameters using the SELECT keys to choose the desired values. For example, if a 76.8 Kbps, synchronous modem is to be tested a typical set-up is shown in figure 3-6.

11. If any difficulty is encountered in changing parameters, use the UP key to scroll up to the SYSTEM CONFIGURATION menu shown in figure 3-5. Ensure that the Function Status is UNLOCKED by pressing the MASTER UNLOCK key located immediately to the right of the CRT and opposite the MASTER UNLOCK display block.

12. Once the desired test set-up parameters have been selected use the down MENU key to return to the MAIN BERT DISPLAY. Using the CURSOR keys to scroll around the display move the highlighted block over the EVENT TIMER and then the FREQUENCY blocks. Use the SELECT keys to set the appropriate parameters to be measured. The possible choices are listed in figure 3-6. For example, if a synchronous system is being tested it is usually a good idea to monitor the received clock so you would select RC in the FREQUENCY block. Similarly, in an Asynchronous test, you would select BR for baud rate.

13. The Model 5500 makes all of its measurements simultaneously but can display only 8 (12 with T1 modules) parameters at a time in the data display blocks. The user may freely program the blocks to display any parameters of interest. This is accomplished by using the CURSOR and SELECT keys as in previous steps. NOTE: Any of the measured parameters may be called up for display while a test is running without losing any data. The choices and their descriptions are shown in figure 3-6.

14. The operator may now begin testing the unit under test by ensuring that the Model 5500 is in correct mode (DCE to test terminal equipment, DTE to test modems) and pressing the RUN key in the upper left next to the CRT.

15. When running, the RUN and SYNC LED's will be lighted if the unit is operating properly.

16. If a problem is detected on power up in the Model 5500 the unit defaults to the SYSTEM CONFIGURATION menu and flashes a FAIL indication next to the defective area identified by the built-in test equipment. (Note: An invalid indication in the USER PROGRAM or USER PATTERN areas may simply mean that nothing has been stored in these memory areas or that the RAM retention battery has discharged.)

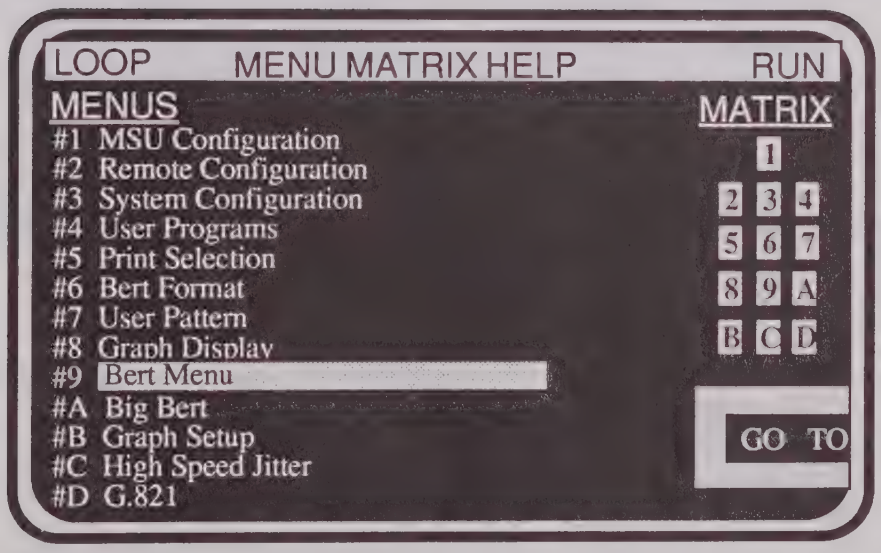


Figure 3-3. MENU MATRIX HELP Display

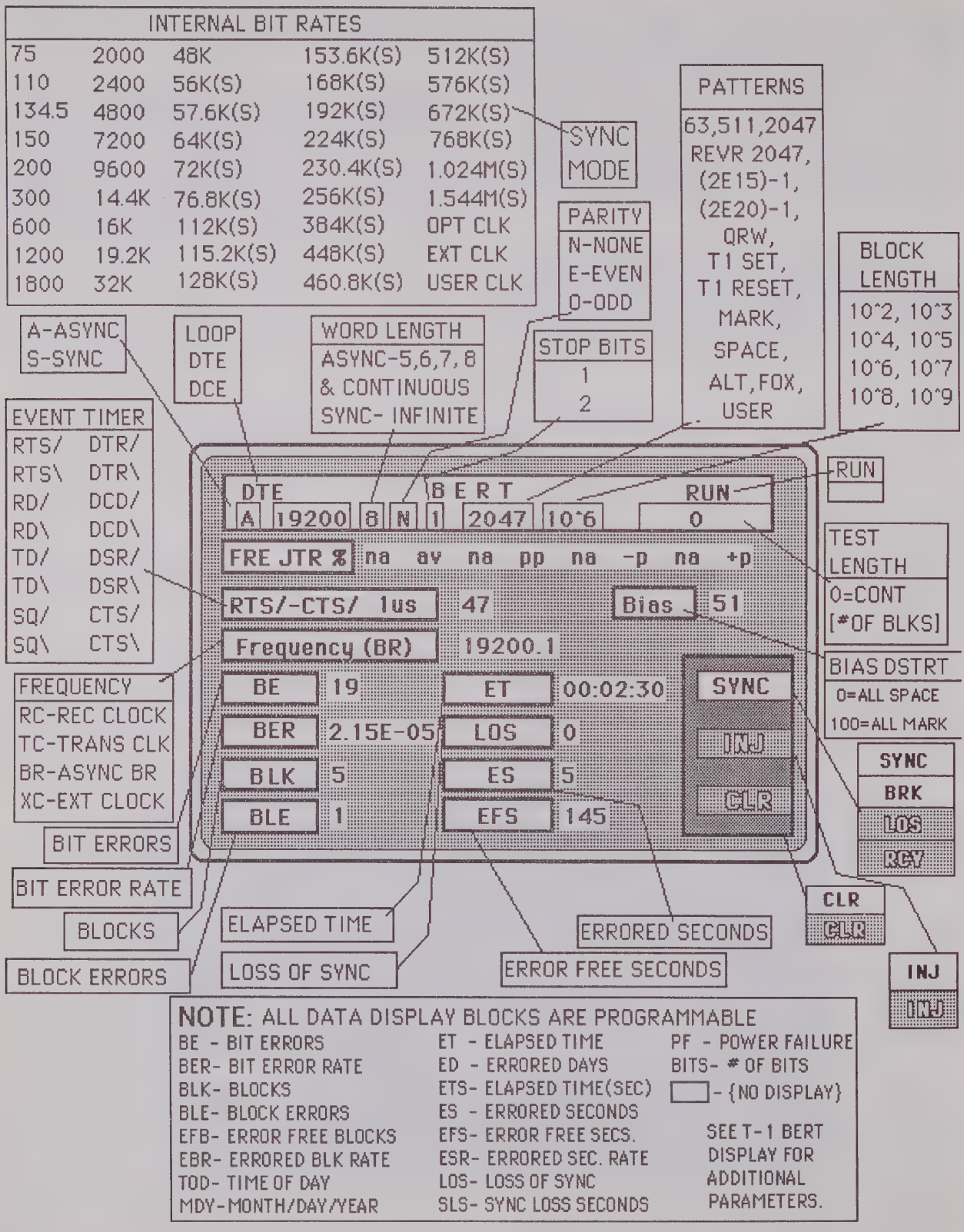


Figure 3-4. BERT Menu

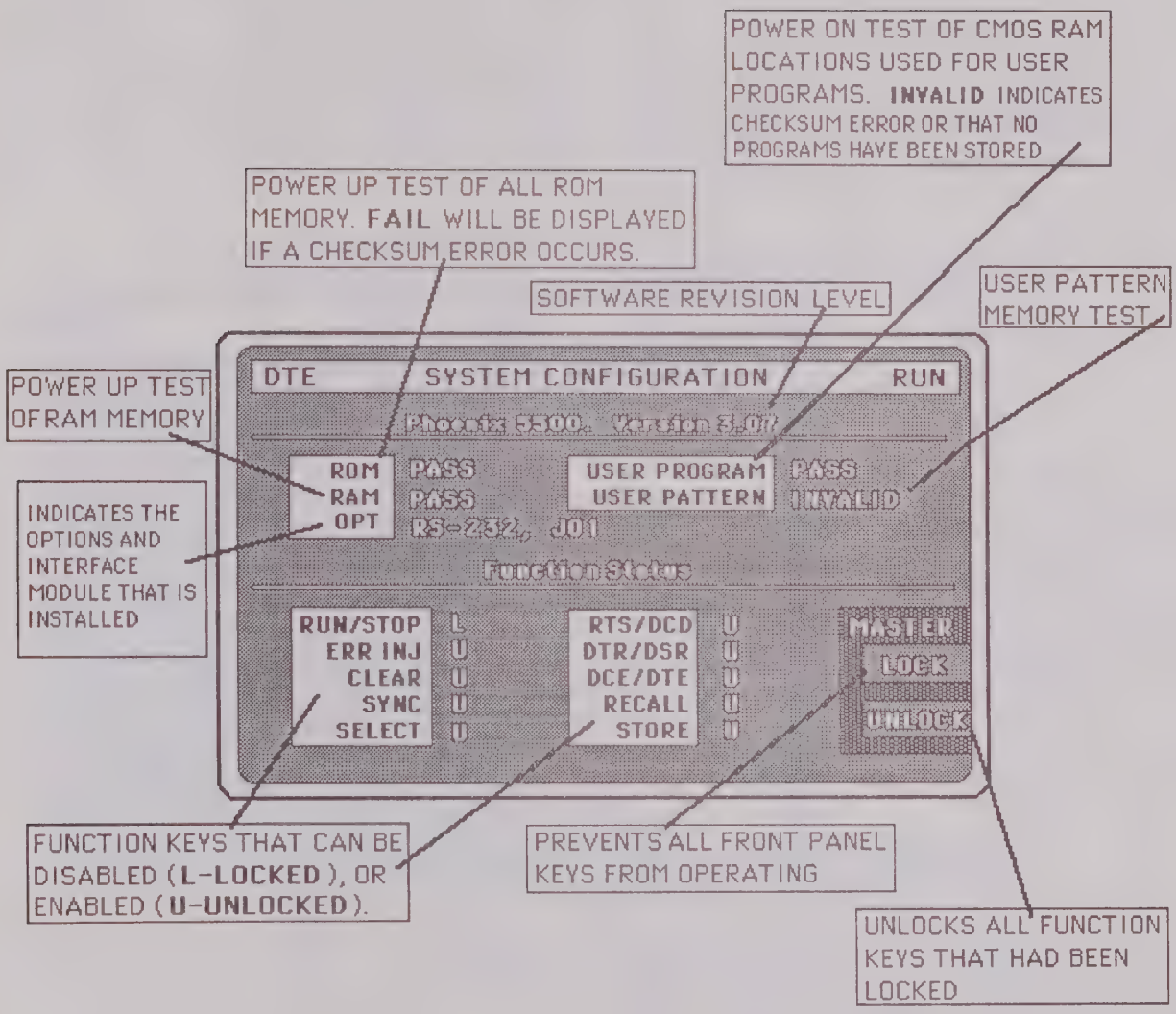

POWER ON TEST OF CMOS RAM LOCATIONS USED FOR USER PROGRAMS. INVALID INDICATES CHECKSUM ERROR OR THAT NO PROGRAMS HAVE BEEN STORED
POWER UP TEST OF ALL ROM MEMORY. FAIL WILL BE DISPLAYED IF A CHECKSUM ERROR OCCURS.
SOFTWARE REVISION LEVEL
USER PATTERN MEMORY TEST
POWER UP TEST OF RAM MEMORY
DTE
SYSTEM CONFIGURATION
RUN
ROM PASS
RAM PASS
OPT RS-232, J01
USER PROGRAM PASS
USER PATTERN INVALID
INDICATES THE OPTIONS AND INTERFACE MODULE THAT IS INSTALLED
Function Status
RUN/STOP L
ERR INJ U
CLEAR U
SYNC U
SELECT U
RTS/DCD U
DTR/DSR U
DCE/DTE U
RECALL U
STORE U
MASTER
LOCK
UNLOCK
FUNCTION KEYS THAT CAN BE DISABLED (L-LOCKED), OR ENABLED (U-UNLOCKED).
PREVENTS ALL FRONT PANEL KEYS FROM OPERATING
UNLOCKS ALL FUNCTION KEYS THAT HAD BEEN LOCKED

Figure 3-5. System Configuration

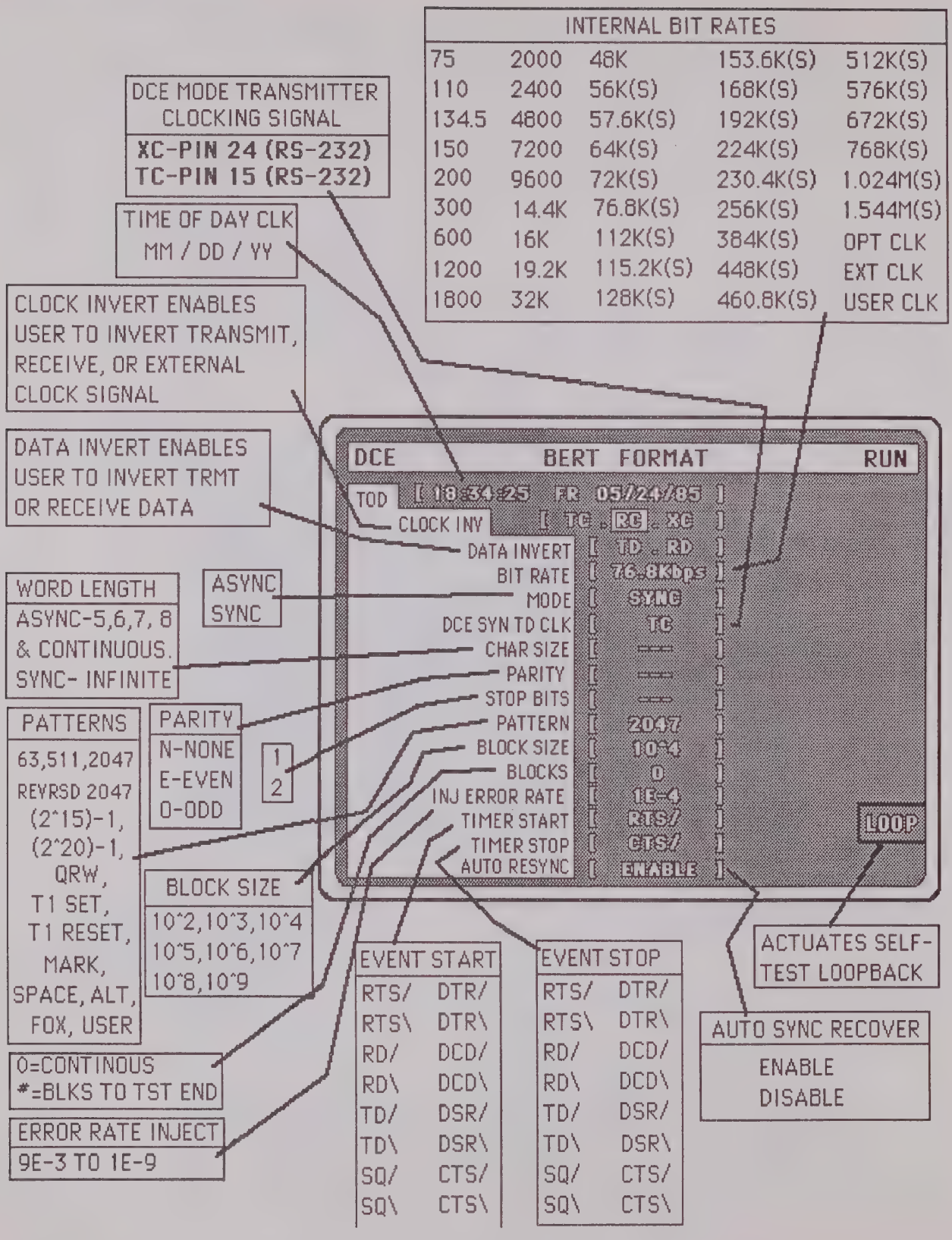


Figure 3-6. BERT Format

3.3.3 GRAPH

The GRAPH DISPLAY, figure 3-8, and its setup menu, GRAPH DATA SELECTION, figure 3-7, occupy the lower left corner of the menu matrix. They are located in locations 8 and B respectively.

3.3.3.1 GRAPH DATA SELECTION

The GRAPH DATA SELECTION menu, figure 8A, allows the user to select (1) data types to be graphed and (2) graphs to be printed. Any or all of the data types shown may be selected for graphing, and any data that is selected for graphing may also be selected for graph printing. The options displayed for each data item are as follows:

"- -" This data item not selected for graphing or printing.

"G -" This data item selected for graphing but not graph printing.

"GP" This data item is selected for both graphing and graph printing.

The SAMPLE PERIOD field defines the sample resolution for the stored graph data. The resolutions available are 1 second, 10 seconds, 1 minute, 10 minutes, and 1 hour. Graph data can be displayed at the sample resolution or the next 2 resolutions, which is selected on the GRAPH DISPLAY menu, figure 3-8.

The PRINT RESOLUTION defines the resolution of the printed graph data. The graph can be printed at the sample resolution or the next two resolutions as summarized below:

Sample Resolution	Print Period may be
1 second	1 or 10 seconds, or 1 minute
10 seconds	10 seconds, or 1 or 10 minutes
1 minute	1 or 10 minutes, or 1 hour
10 minutes	10 minutes or 1 hour
1 hour	1 hour

The SELECT and CANCEL SoftKeys will either select (activate) or cancel any changes made on the GRAPH DATA SELECTION menu. These key labels will flash to indicate that the stored configuration and the graph data do not match the displayed configuration.

NOTE: Pressing SELECT will activate the new configuration and discard any stored graph data. Pressing CANCEL will cancel any changes made and redisplay the previous selections without discarding the stored graph data.

3.3.3.2 GRAPH DISPLAY MENU

The GRAPH DISPLAY menu, figure 8, displays a single graph for any of the data types selected on the GRAPH DATA SELECTION menu. The data type indicated at the top of the screen may be changed to select a particular graph.

The HORIZ and VERT fields select the horizontal and vertical resolution for the displayed graph. The horizontal resolution is a function of the sample period as defined above for the print resolution. The vertical resolution selects a magnitude multiplier corresponding to the labels on the left side of the graph. The horizontal resolution is common to all data types, but each data item may have a unique vertical resolution.

THE CRSR1 and CRSR2 define the day-of-week, hour, and minute of the samples at cursors 1 and 2. The two cursors may be used to print a section of the graph data. Cursor 2 may be OFF; if not, cursor 1 always precedes cursor 2.

MAG1 and MAG2 display the magnitudes of the data at cursors 1 and 2.

The graph data buffer is approximately 5400 samples long. Data is collected and stored until the buffer fills, and then the oldest sample(s) are discarded as required to make room for the new samples. The period of time that is represented by data in the buffer is a function of the sample period and the number of data types to be sampled. For example, assume a sample period of 10 seconds with three data types selected. To compute buffer length:

Buffer Length = (5400/3)*10 = 18,000 seconds = 5 hours.

3.3.4 Program Storage and Recall

1. Once the model 5500 has been configured for a particular test and the menu displays are set to the operator's satisfaction press the STORE key located in the lower right hand corner of the front panel and the Model 5500 stores all of the menu setups and display parameters. The 5500 will store up to ten different tests.

2. After pressing the STORE key the unit will immediately default to the USER PROGRAM menu. The USER STORED PROGRAM menu is located in the upper right corner of the menu matrix. If nothing has been stored or labeled, the user can number the test set up any way desired. This is done by pressing the desired number on the HEX keypad located next to the SELECT keys after pressing the STORE key.

3. In summary, the program storage function is a two step process; 1) press STORE and then, 2) press a number from 0 to 9.

NOTE: To label a stored program it is easier to type in the label using a keyboard terminal connected to the remote control port. If a keyboard terminal is not available, the labeling may be accomplished from the front panel.

4. Using the MENU cursor keys scroll to the upper right hand corner menu labeled USER STORED PROGRAM. Refer to figure 3-9 for a sample menu.

5. If necessary scroll to the highlighted block opposite the number of the program stored.

6. The complete character set (upper and lower case) is available by using SELECT keys to scroll to the desired character.

7. The user must move the block one place to the right and repeat the procedure to enter each character in the program name. For example Program 0 may have been a 1200 bps, async test on a 212 type modem.

The user might label the program : 212 MODEM TEST.

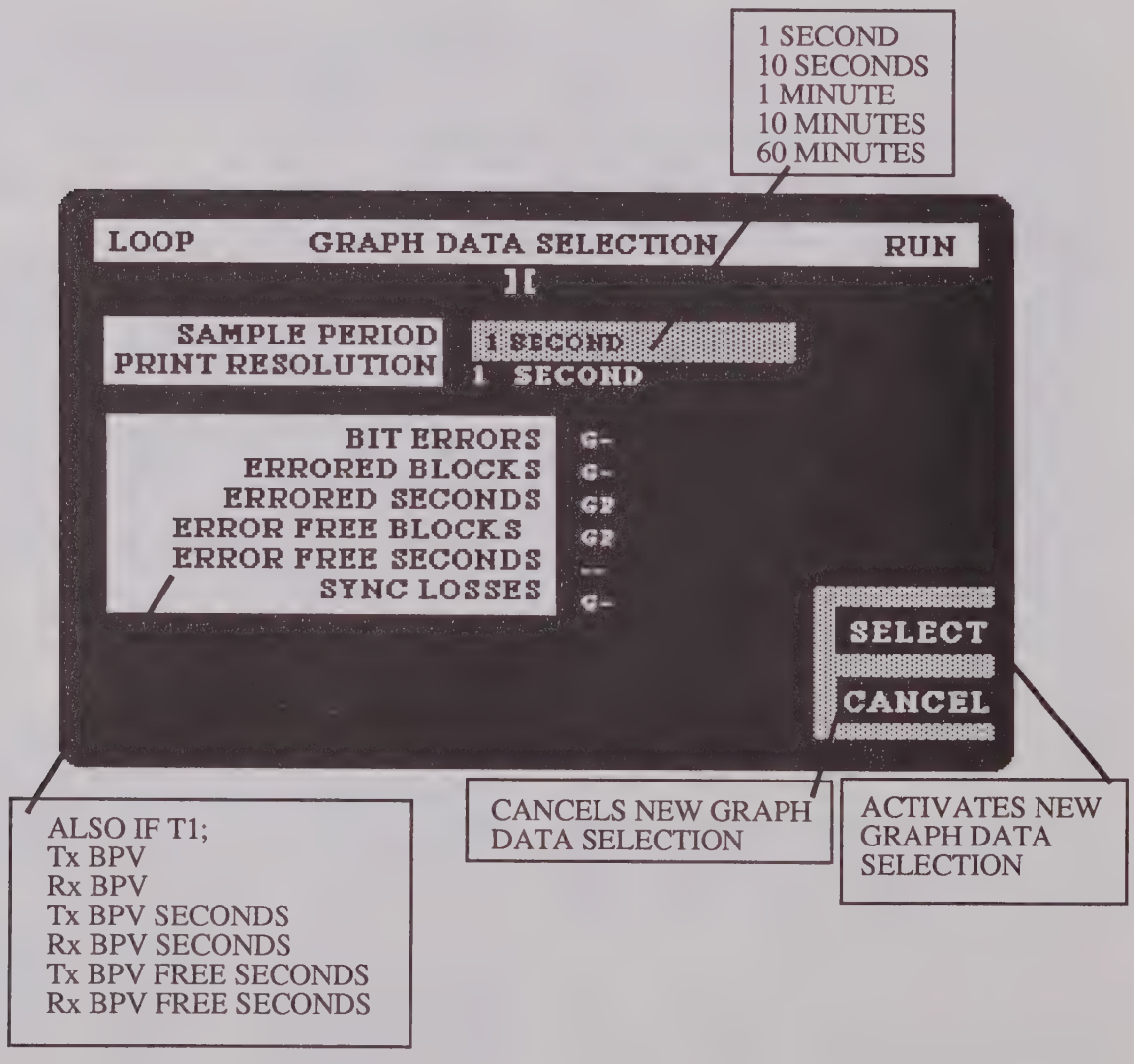


Figure 3-7. 5500 GRAPH DATA SELECTION Menu

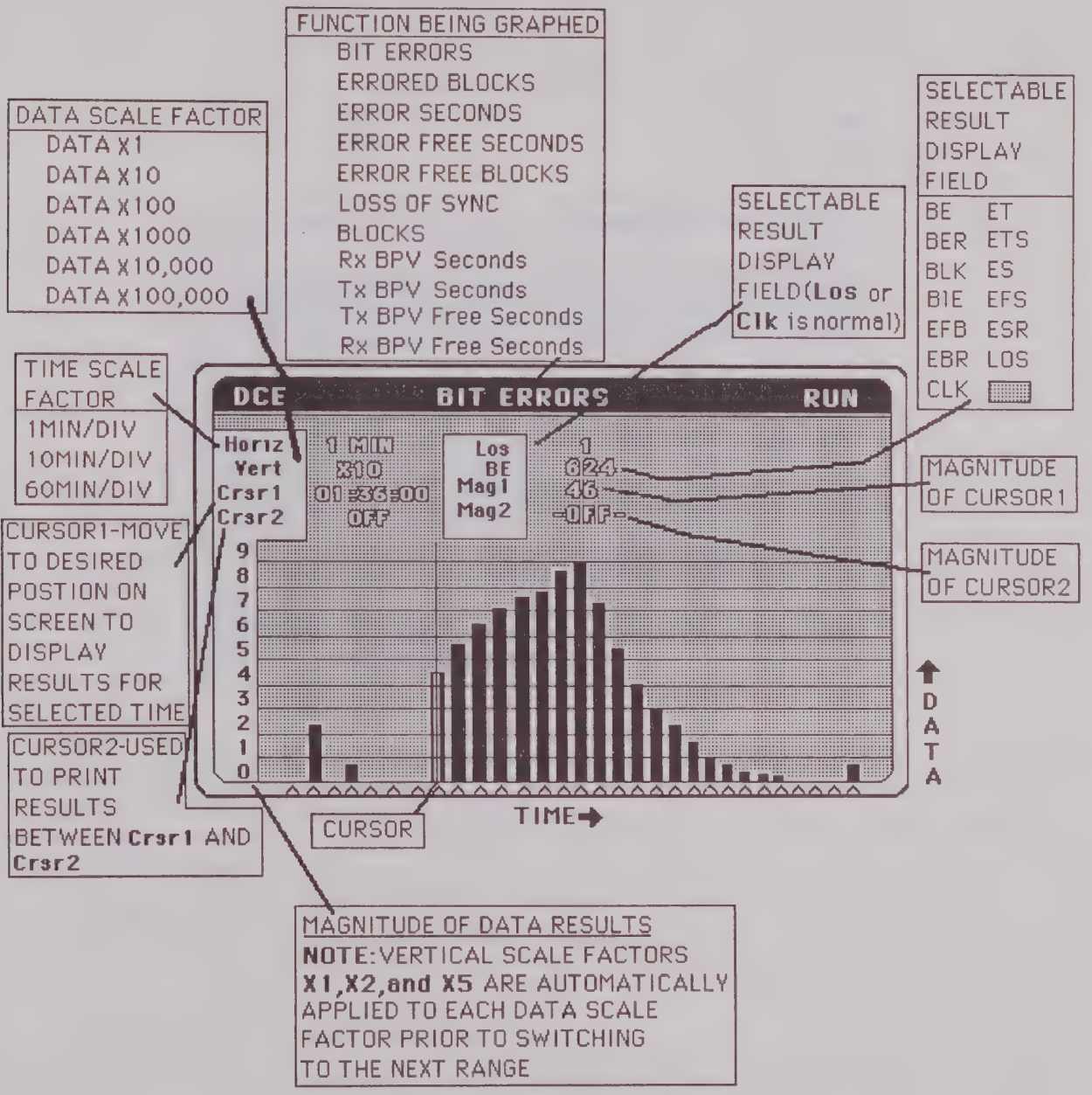


Figure 3-8. 5500 GRAPH Display

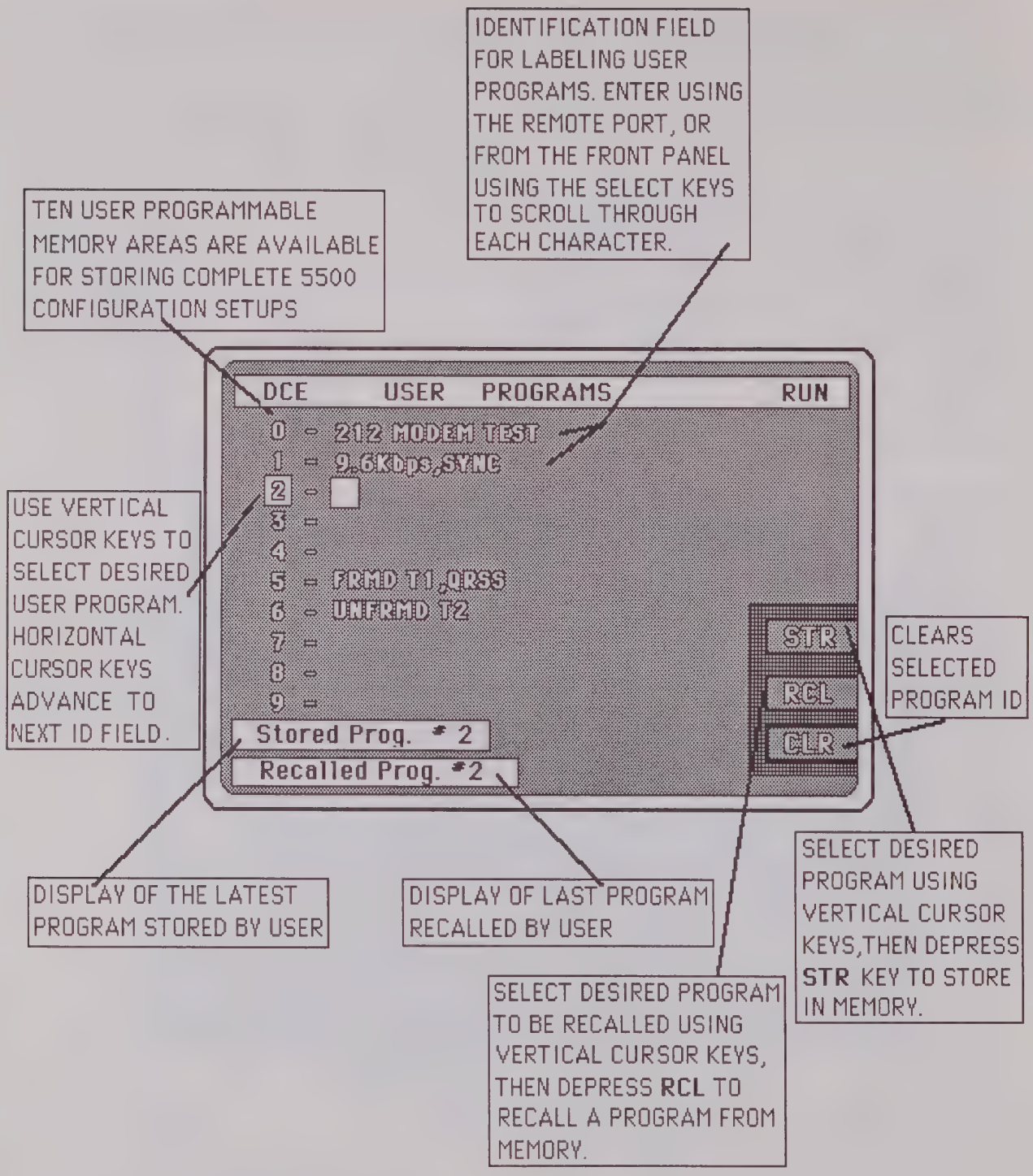

IDENTIFICATION FIELD FOR LABELING USER PROGRAMS. ENTER USING THE REMOTE PORT, OR FROM THE FRONT PANEL USING THE SELECT KEYS TO SCROLL THROUGH EACH CHARACTER.
TEN USER PROGRAMMABLE MEMORY AREAS ARE AVAILABLE FOR STORING COMPLETE 5500 CONFIGURATION SETUPS
DCE USER PROGRAMS RUN
0 = 212 MODEM TEST
1 = 9.6Kbps,SYNC
2 =
3 =
4 =
5 = FRMD T1,QRSS
6 = UNFRMD T2
7 =
8 =
9 =
STR
RCL
CLR
Stored Prog. # 2
Recalled Prog. #2
USE VERTICAL CURSOR KEYS TO SELECT DESIRED USER PROGRAM. HORIZONTAL CURSOR KEYS ADVANCE TO NEXT ID FIELD.
CLEARS SELECTED PROGRAM ID
SELECT DESIRED PROGRAM USING VERTICAL CURSOR KEYS,THEN DEPRESS STR KEY TO STORE IN MEMORY.
DISPLAY OF THE LATEST PROGRAM STORED BY USER
DISPLAY OF LAST PROGRAM RECALLED BY USER
SELECT DESIRED PROGRAM TO BE RECALLED USING VERTICAL CURSOR KEYS, THEN DEPRESS RCL TO RECALL A PROGRAM FROM MEMORY.

Figure 3-9. 5500 USER PROGRAM Display

8. Once the test programs have been stored they can be recalled by pressing RECALL twice. This causes the unit to default to the USER PROGRAM menu. Then press the number (0-9) of the desired test program.

NOTE: It is implicit that the user has placed the correct interface module into the Model 5500. That is, the user should not expect to perform T-1 tests with an RS-232 module plugged in the 5500.

9. The operator may overwrite a stored program by storing a new program on top of the old one.

10. The operator may store and recall programs from the USER PROGRAM menu by using the "soft keys" labeled STR and RCL in the same way the STORE and RECALL keys are used.

11. The CLEAR key is used to blank the program label on the current line.

3.3.5 Remote Port - RS-232

1. The RS-232 remote port also functions as the printer port. It is possible to configure the port to look at either modems or terminal equipment by removing the top cover and changing the dip switches as outlined in section 2 of this manual.

2. The Model 5500 is shipped from the factory with its RS-232 port configured as a DCE. That is, it is emulating a modem expecting a printer or terminal to be connected to it.

3. If it is desired to connect a Modem to the port then a modem eliminator cable must be used, or the dip switches within the unit must be changed to "DTE" position. Refer to section 2 of this manual for instructions regarding this change.

4. To configure the remote port the the operator must use the MENU keys to scroll to the upper left hand corner display, the REMOTE PORT CONFIG menu.

5. The REMOTE PORT CONFIG menu, shown in figure 3-10, enables the user to match any asynchronous modem, terminal, or printer operating over the 50 bps to 9600 bps range.

6. The user selects RS-232 or PRINTER using the "soft keys" located beside the CRT. Select RS-232 if Terminal or Modem operation is desired. Select PRINTER when using a direct printer connection.

7. The user must then select the bit rate, character size, parity and stop bits to match the serial remote port to the device (DCE or DTE) connected to the remote port.

8. The TRACE mode, if enabled, allows the user to review the data stream coming and going over the serial port for possible troubleshooting.

9. The user must also select either the Carriage Return Line Feed or ACK-NAK handshake protocol applicable to the equipment attached to the serial port.

10. The Model 5500 is now be ready for printer or remote operation.

3.3.6 Remote Port - IEEE-488

1. The parallel IEEE-488 remote port is similar in operation to the RS-232 serial port and is selected from the same menu.

2. IEEE-488 (sometimes referred to as GPIB or HPIB) is selected using the "Soft Key" labeled IEEE-488 on the CRT.

3. The user selects the handshake protocol as CR-LF or ACK-NAK as appropriate.

4. The IEEE-488 Bus, enables the simultaneous connection of up to 31 instruments to single controller. The system operates by prefacing each data packet with an address. It is thus necessary for the user to select a numeric address (0-30) for the Model 5500. Then it will "listen" on the bus and respond to any commands prefaced by its address.

3.3.7 Printer

1. The remote port must be configured and the printer connected as described above.

2. Select the BERT PRINT MENU (As shown in figure 3-2, the BERT PRINT MENU is located immediately above the GRAPH DISPLAY). Scroll to the BERT PRINT MENU using the MENU cursor keys.

3. When in the BERT PRINT MENU, figure 3-7, the user selects either numeric data or the graphic display to print.

4. In order to print the graphic display it is necessary to have a graphics capable printer such as the Model 5500-P01, EPSON RX-80, LX-80, or equivalent.

5. Numeric data may be printed on any serial printer compatible with the Model 5500 async remote port data format.

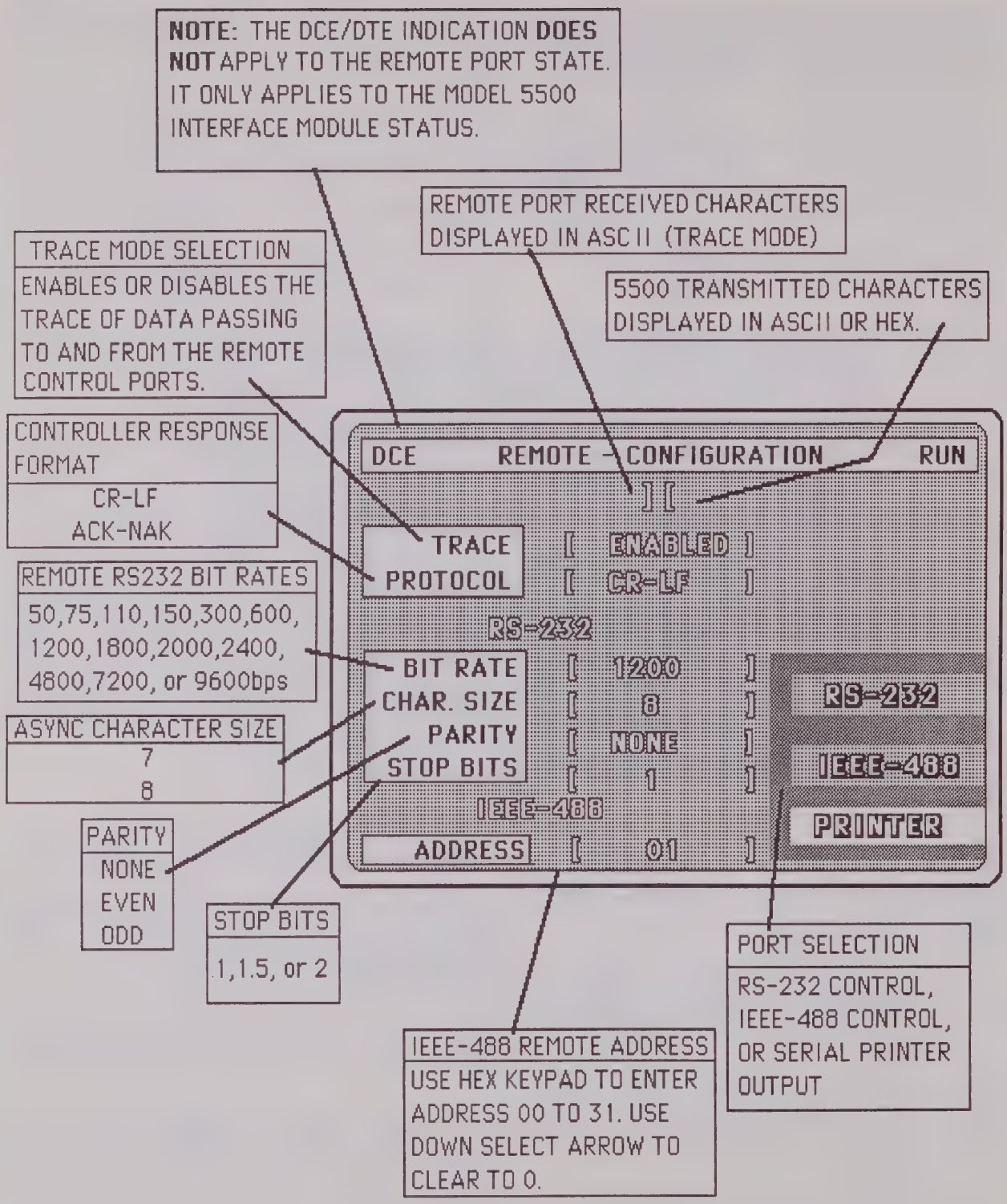

NOTE: THE DCE/DTE INDICATION DOES NOT APPLY TO THE REMOTE PORT STATE. IT ONLY APPLIES TO THE MODEL 5500 INTERFACE MODULE STATUS.
REMOTE PORT RECEIVED CHARACTERS DISPLAYED IN ASCII (TRACE MODE)
5500 TRANSMITTED CHARACTERS DISPLAYED IN ASCII OR HEX.
TRACE MODE SELECTION
ENABLES OR DISABLES THE TRACE OF DATA PASSING TO AND FROM THE REMOTE CONTROL PORTS.
CONTROLLER RESPONSE FORMAT
CR-LF
ACK-NAK
REMOTE RS232 BIT RATES
50,75,110,150,300,600, 1200,1800,2000,2400, 4800,7200, or 9600bps
ASYNC CHARACTER SIZE
7
8
PARITY
NONE
EVEN
ODD
STOP BITS
1,1.5, or 2
DCE REMOTE - CONFIGURATION RUN
TRACE [ENABLED]
PROTOCOL [CR-LF]
RS-232
BIT RATE [1200]
CHAR. SIZE [8]
PARITY [NONE]
STOP BITS [1]
IEEE-488
ADDRESS [01]
RS-232
IEEE-488
PRINTER
IEEE-488 REMOTE ADDRESS
USE HEX KEYPAD TO ENTER ADDRESS 00 TO 31. USE DOWN SELECT ARROW TO CLEAR TO 0.
PORT SELECTION
RS-232 CONTROL, IEEE-488 CONTROL, OR SERIAL PRINTER OUTPUT

Figure 3-10. 5500 Remote Port Display

6. If graphic data is selected the user may select the entire graph for printing or only the data between CRSR 1 and CRSR 2. The selection is made using the "soft keys" beside the CRT.

7. If the Data Mode is chosen then any or all of the numerical results of the parameter measurements will be printed according to conditions selected by the user.

8. The user moves the cursor highlight to the DATA PRINT CONDITIONS field and using the SELECT keys chooses the conditions under which a print out will occur. For example, the user may want a print out to occur every hour, whenever a bit error occurs, or if there is a power failure.

9. Having chosen up to a maximum of four conditions, the user will then obtain a print whenever any or all of the chosen conditions occur.

10. The user must also select what data he wants printed. Use the cursor keys to scroll to the appropriate parameters and use the SELECT keys to enter an "X" in the desired parameter's block. A "-" will delete that parameter from the print out.

3.4 MENU DESCRIPTIONS

The basic Model 5500 has thirteen different screen menus arranged as shown in figure 3-2 and 3-3. The menus along the bottom two rows are those used to display test results while the remaining seven menus are used for setting up the tests or print functions, storing programs or user patterns, or reviewing system status. The seven menus are rarely used once the operator has set up the Model 5500 to suit his testing requirements. A description of each menu and its functions follow.

3.4.1 Main BERT Menu

This is the primary test menu used while running a Bit Error Rate Test (BERT). This display comes up after the power is turned on if the unit is operating correctly. All numerical test results are simultaneously measured and 8 may be displayed on the CRT. The Model 5500 measures up to 25 different parameters simultaneously and enables the user to select up to eight of them for display at any time. The T-Carrier and CCITT G.703 module options permit the user to display up to twelve parameters at any time. It is important to note that while the unit may display only eight or twelve parameters at a time the other parameters are still being measured and results accumulated. They can be called up at any time without interrupting or disturbing any test in progress.

The key control setups for bit error testing are located at the top of the display screen. The user is able to see and change the test settings live during testing without stopping the test. The current mode of operation (DCE or DTE) is also displayed in the upper left hand corner of the display.

The display parameters, test parameter options, and their locations on the CRT are shown in figure 3-4. Note that in addition to bit error test data, the MAIN BERT DISPLAY shows Bias Distortion on the received data, frequency measurement of synchronous receive, transmit or external clocks or asynchronous baud rate, between any two interface control line signal occurrences, and optional edge jitter (isochronous distortion). Bias Distortion or Skew is the ratio of Marks (1's) to Spaces (0's) expressed as a percentage. Event time provides a measure of the time between such event occurrences as RTS leading edge to CTS leading edge or DTR leading edge to DSR leading edge with up to 1 microsecond resolution.

The MAIN BERT DISPLAY menus for T-Carrier and CCITT G.703 interface modules differ slightly since the Bias Distortion, Event Time, and Optional Edge Jitter measurements are not required for these interfaces, Measurements at these interfaces are discussed in detail in the later sections of this manual.

3.4.2 BERT Format Menu

The BERT FORMAT MENU shown in figure 3-6 and located directly above the main BERT DISPLAY, contains all of the test set up parameters to set up Bit Error Testing. The parameters are spelled out in this menu as opposed to the MAIN BERT DISPLAY where the set up parameters at the top of the menu are not. The set up parameters can, of course, be changed from either menu. The BERT FORMAT MENU allows the user to set up a larger number of parameters. For instance, the operator can set the time date, week, month and year. The polarity of the data and clock signals may also be inverted independently. The clock source for synchronous Transmit Data on the DCE mode can be selected as internal (TC-pin 15 (RS-232)) or external (XC-pin 24 (RS-232)).

The BERT FORMAT MENU also enables the user to actuate the built in loopback self test function. The soft key opposite the LOOP block causes the Model 5500 to loop the data and clocks back in order to test itself. This function is used if the operator suspects a malfunction in the Model 5500.

Another feature of the Model 5500 is it's ability to reverse the 2047 bit length pseudo-random pattern. This is to accommodate certain embedded equipments which incorporate this non-standard pattern. The PATTERN block will display this as REV 2047 or 2047 R

depending upon whether it is shown on the BERT FORMAT MENU or the MAIN BERT DISPLAY menu.

3.4.3 Graph Display

The GRAPH DISPLAY, shown in figure 3-8, may be used to plot selected Bit Error test data parameters. The basic GRAPH DISPLAY is capable of storing up to 60 hours of data in 1 minute intervals. The following data may be plotted (if selected on the GRAPH DATA SELECTION menu):

Bit Errors	T1
Errored Blocks	Tx BPV
Errored Seconds	Rx BPV
Error Free Seconds	Tx BPV Seconds
Errored Free Blocks	Rx BPV Seconds
Sync Losses	Tx BPV Free Seconds
	Rx BPV Free Seconds

The GRAPH DISPLAY allows the user to choose a convenient Horizontal and Vertical scale factor. As an example, let us assume that bit errors are being graphed (no other parameters are being graphed). A convenient horizontal scale may be one minute per division with a vertical scale setting of X1. These are sensitive scale factors and even the occurrence of one bit error will not go unnoticed. As experience with the system under test is accumulated, the operator may change the scale factors to less sensitive values in order to keep the display on the CRT.

NOTE: The scale factors can be changed at any time without loss of data.

For convenience, the user is also free to select and display any two of the data parameter's numerical results in the SELECTABLE DISPLAY RESULT field to the right of the HORIZ and VERT Scale factor fields.

This is particularly convenient for observing the total accumulated bit errors while watching errors at a particular time on the graph. The user may also look at sync losses, block errors or any other parameters of interest.

The Model 5500 can graph up to 60 hours of data in 1 minute intervals for one parameter. It would be inconvenient to try to count over to a particular time by hand. Instead, two CURSORS can be moved over to the point of interest and give time and magnitude of the event.

This is accomplished by using the CURSOR to place the half intensity block over either CRSR 1 or CRSR 2 as desired. Then, using the SELECT keys, scroll the CRSR desired over the point of interest. CRSR 2 is always beneath CRSR 1 so moving CRSR 1 will move both cursors. When CRSR 1 has been placed in position move the half intensity block down to CRSR 2 then the SELECT keys can move CRSR 2 to the right of CRSR 1. Note that CRSR 2 cannot go behind CRSR 1.

3.4.4. Graph Data Selection

The data parameters to be graphed are chosen from the list on the GRAPH DATA SELECTION menu as shown in figure 3-7. The CURSOR key is used to move the half intensity block over the data field and the SELECT keys then choose "- -", "G -", or "GP" as desired.

3.4.5. Print Menu

The PRINT MENU display, figure 3-11, located above the GRAPH DISPLAY is used to set up; the conditions under which a print out will occur; what is to be printed out; and whether it is to be numerical data or a graphical presentation. This menu enables the user to customize the test results printout for the parameters, and only those parameters, of interest. This printout of data itself may be set to occur based upon time, blocks, errors, bipolar violations (T-1), end of test, or power failure.

The user may enable either GRAPH, DATA, or both printouts. The Model 5500 is compatible with most standard serial RS-232 printers. The printer port can be configured to accommodate the data format of virtually any serial printer. It is necessary to configure the RS-232 serial port to match the data format of the printer. This is covered in the Remote Port menu description, section 3.4.8 of this manual.

3.4.6 System Configuration

The SYSTEM CONFIGURATION MENU, figure 3-5, serves a dual purpose. On power up, the Model 5500 performs a self test function. The unit will default to the System Configuration menu if an abnormal condition is detected. In the case of a fault detection, the problem area will be "flashed". The unit checks Read Only Memory (ROM), Random Access Memory (RAM), User Program and User Pattern memory. It also tells the user which Inter-face Module option is plugged in.

The System Menu also enables the user to "lock-out" any or all of the front panel operation keys.

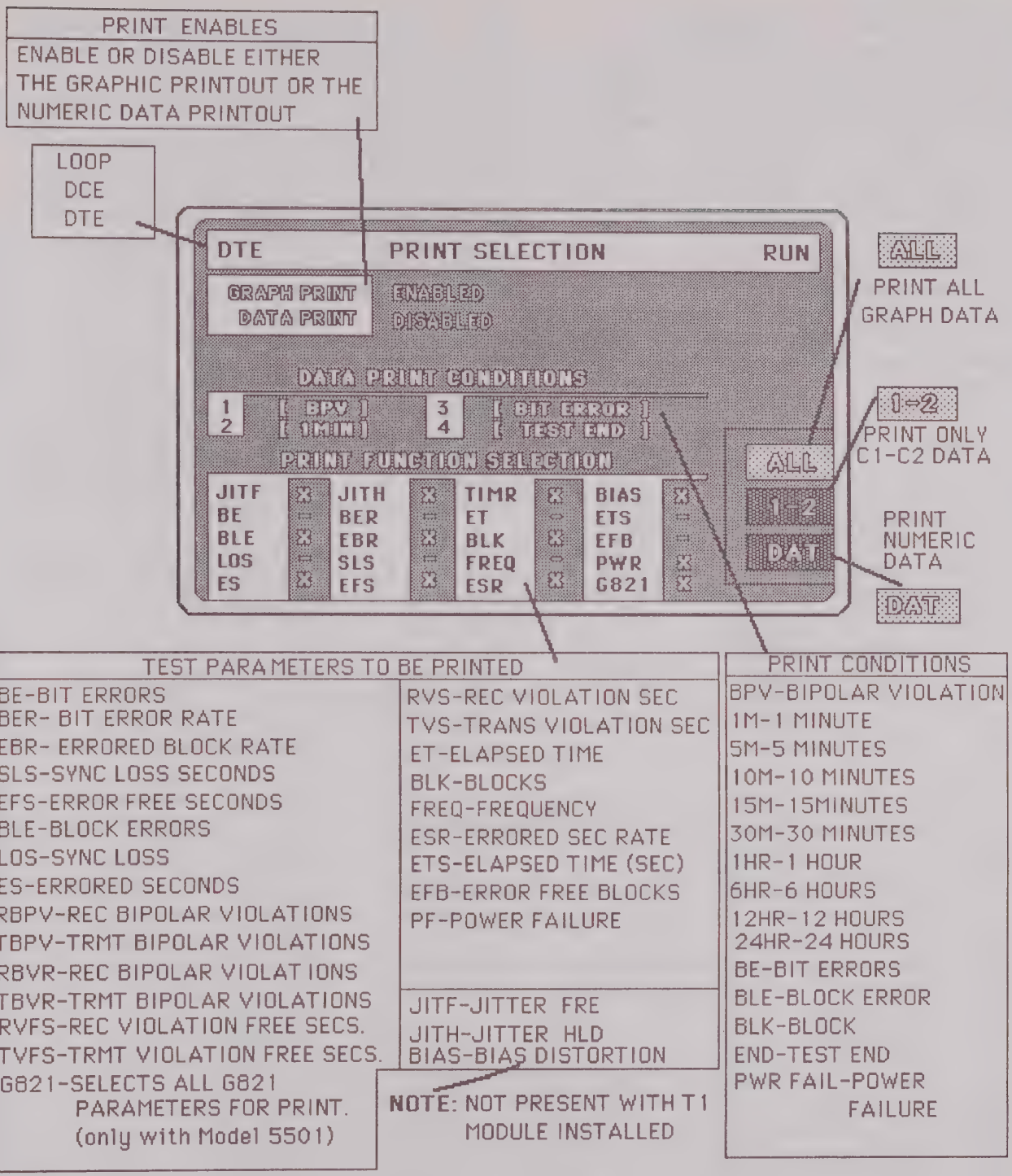


Figure 11. 5500 PRINT Menu

An individual function, such as RUN/STOP, may be locked out by using the CURSOR to place the half intensity block over the function and pressing either SELECT key. This is shown in figure 3-5. However, by using the "soft keys" located beside the lower right hand corner of the CRT, it is possible to lock out or unlock all of the front panel keys at once. Pressing the soft key opposite the LOCK display block will cause all keys to be locked out and highlights the block.

NOTE: The user is still able to use the MENU cursor keys to scroll around and review the various menus. However, the user cannot change any of the parameters, stop a test, clear results, or change any of the parameters, or change operating modes when the unit has been locked.

3.4.7 User Pattern

The USER PATTERN display, figure 3-12, allows the user to construct patterns for transmission by the Model 5500. The USER PATTERN selection, when chosen, causes the Model 5500 to transmit a repetitive pattern of whatever the operator has placed in the USER PATTERN display. The user is permitted to enter up to 135 characters in HEX from the front panel HEX keypad or over the Remote Control ports. Each character in HEX is an 8 bit long word so the total bit length which could be input is 1080 bits. However, the user may enter as few as three characters if desired.

NOTE: If the RAM backup battery failed or has been replaced it is possible that the Model 5500 will, power up, default to the system menu and flash the USER PATTERN memory block. This "error" can be ignored or the user may choose to place three or four characters into the User Pattern display. These can be any HEX characters or the user may want to place an actual pattern into memory.

Placing a HEX pattern into a memory is a straight forward process. The user scrolls to the USER PATTERN display using the MENU keys. Then, beginning in the upper left hand corner, enters the desired HEX character from the HEX keypad. Using the Right CURSOR key, advance the half intensity block to the next position and enter another character. Repeat this process for the pattern length desired.

The user may desire to input a pattern on a binary, bit by bit basis. This is a somewhat more complex procedure, but the following table and examples will serve to explain the procedure

Table 3-2 contains the 256 possible HEX combinations and their binary equivalents.

Table 3-2. HEX to Binary Conversion

HEX	BINARY (LSD)	HEX	BINARY (LSD)	HEX	BINARY (LSD)
00	00000000	50	00001010	A0	00000101
01	10000000	51	10001010	A1	10000101
02	01000000	52	01001010	A2	01000101
03	11000000	53	11001010	A3	11000101
04	00100000	54	00101010	A4	00100101
05	10100000	55	10101010	A5	10100101
06	01100000	56	01101010	A6	01100101
07	11100000	57	11101010	A7	11100101
08	00010000	58	00011010	A8	00010101
09	10010000	59	10011010	A9	10010101
0A	01010000	5A	01011010	AA	01010101
0B	11010000	5B	11011010	AB	11010101
0C	00110000	5C	00111010	AC	00110101
0D	10110000	5D	10111010	AD	10110101
0E	01110000	5E	01111010	AE	01110101
0F	11110000	5F	11111010	AF	11110101

Table 3-2. HEX to Binary Conversion (Cont)

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
10	00001000	60	00000110	B0	00001101
11	10001000	61	10000110	B1	10001101
12	01001000	62	01000110	B2	01001101
13	11001000	63	11000110	B3	11001101
14	00101000	64	00100110	B4	00101101
15	10101000	65	10100110	B5	10101101
16	01101000	66	01100110	B6	01101101
17	11101000	67	11100110	B7	11101101
18	00011000	68	00010110	B8	00011101
19	10011000	69	10010110	B9	10011101
1A	01011000	6A	01010110	BA	01011101
1B	11011000	6B	11010110	BB	11011101
1C	00111000	6C	00110110	BC	00111101
1D	10111000	6D	10110110	BD	10111101
1E	01111000	6E	01110110	BE	01111101
1F	11111000	6F	11110110	BF	11111101
20	00000100	70	00001110	C0	00000011
21	10000100	71	10001110	C1	10000011
22	01000100	72	01001110	C2	01000011
23	11000100	73	11001110	C3	11000011
24	00100100	74	00101110	C4	00100011
25	10100100	75	10101110	C5	10100011
26	01100100	76	01101110	C6	01100011
27	11100100	77	11101110	C7	11100011
28	00010100	78	00011110	C8	00010011
29	10010100	79	10011110	C9	10010011
2A	01010100	7A	01011110	CA	01010011
2B	11010100	7B	11011110	CB	11010011
2C	00110100	7C	00111110	CC	00110011
2D	10110100	7D	10111110	CD	10110011
2E	01110100	7E	01111110	CE	01110011
2F	11110100	7F	11111110	CF	11110011
30	00001100	80	00000001	D0	00001011
31	10001100	81	10000001	D1	10001011
32	01001100	82	01000001	D2	01001011
33	11001100	83	11000001	D3	11001011
34	00101100	84	00100001	D4	00101011
35	10101100	85	10100001	D5	10101011
36	01101100	86	01100001	D6	01101011
37	11101100	87	11100001	D7	11101011
38	00011100	88	00010001	D8	00011011
39	10011100	89	10010001	D9	10011011
3A	01011100	8A	01010001	DA	01011011
3B	11011100	8B	11010001	DB	11011011
3C	00111100	8C	00110001	DC	00111011
3D	10111100	8D	10110001	DD	10111011
3E	01111100	8E	01110001	DE	01111011
3F	11111100	8F	11110001	DF	11111011

Table 3-2. HEX to Binary Conversion (Cont)

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
40	00000010	90	00001001	E0	00000111
41	10000010	91	10001001	E1	10000111
42	01000010	92	01001001	E2	01000111
43	11000010	93	11001001	E3	11000111
44	00100010	94	00101001	E4	00100111
45	10100010	95	10101001	E5	10100111
46	01100010	96	01101001	E6	01100111
47	11100010	97	11101001	E7	11100111
48	00010010	98	00011001	E8	00010111
49	10010010	99	10011001	E9	10010111
4A	01010010	9A	01011001	EA	01010111
4B	11010010	9B	11011001	EB	11010111
4C	00110010	9C	00111001	EC	00110111
4D	10110010	9D	10111001	ED	10110111
4E	01110010	9E	01111001	EE	01110111
4F	11110010	9F	11111001	EF	11110111
F0	00001111	F6	01101111	FB	11011111
F1	10001111	F7	11101111	FC	00111111
F2	01001111	F8	00011111	FD	10111111
F3	11001111	F9	10011111	FE	01111111
F4	00101111	FA	01011111	FF	11111111
F5	10101111				

Step 1: Write the pattern desired bit by bit in the following format with the first transmitted bit first. An example T1 set code pattern is shown below (a continual repeating 10000).

1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 ----------

Step 2: Table 3-2 is constructed so that the least significant bit (LSB) is the inverse of what normally would be expected. This is a reference to allow the user to easily "invert" the desired pattern.

Step 3: Segment the pattern into 8 bit bytes as shown below until the pattern repeats. Note that in this example the pattern repeats after the fortieth bit.

10000100 00100001 00001000 01000010 00010000 10000100

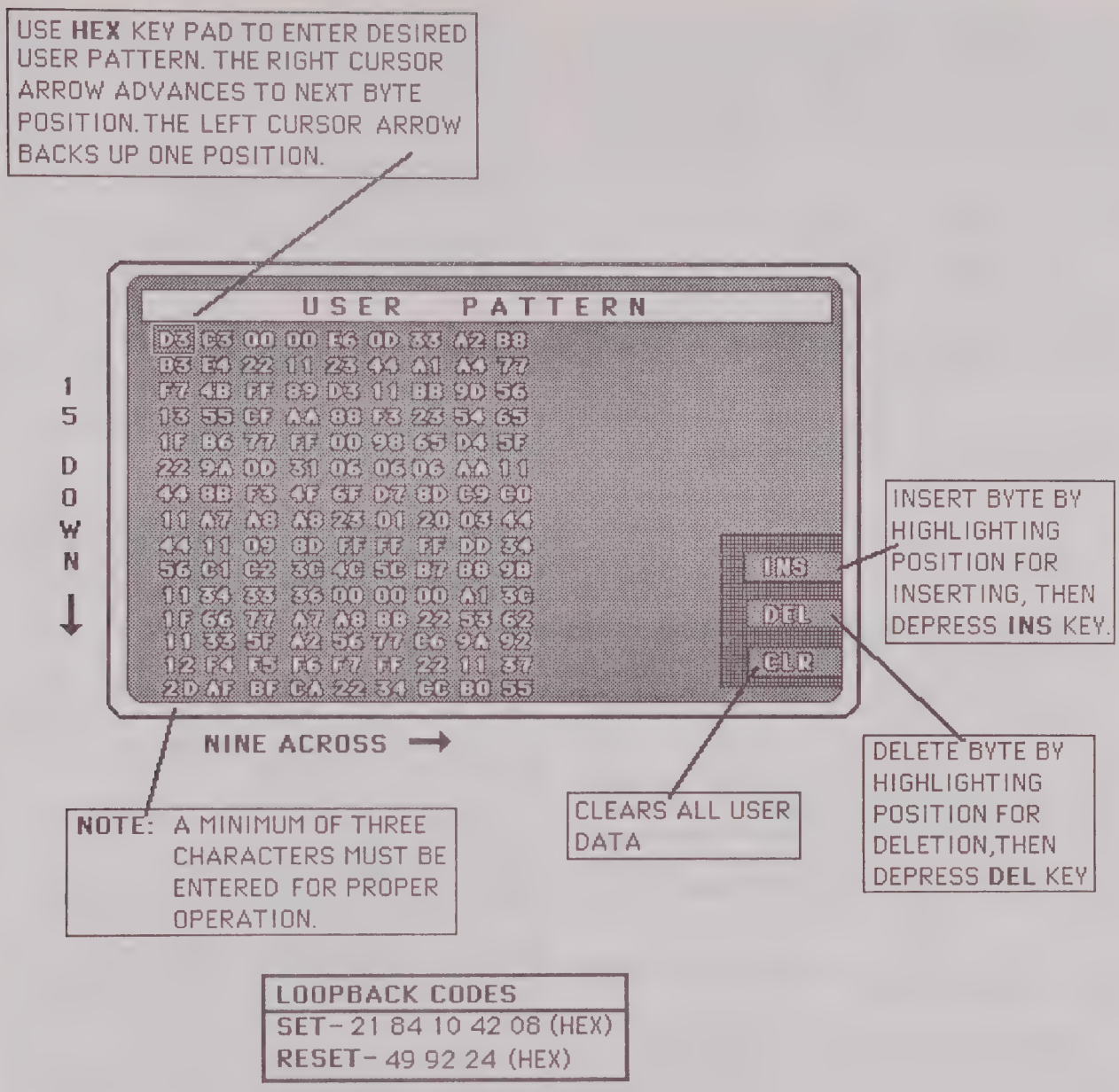
Step 4: Compare the first byte (10000100) to the various bytes in the Table 3-2 and note that it is identical to the pattern for the HEX character set "21".

Step 5: Compare the second byte (00100001) to the tabulated values and note that it is equivalent to HEX "84".

Step 6: Repeat the procedure for all the remaining bytes. Note: that the 40 bit long pattern equates to the HEX character string "21 84 10 42 08".

STEP 7: The repetitive 10000 pattern has thus been converted into its HEX pattern "21 84 10 42 08" into the USER PATTERN display and the pattern generated will be a continuous 1000010000-----.

NOTE: This sample pattern (10000) is the Set Code used to loop back a T-1 Channel Service Unit (CSU) such as the Phoenix Model 1544.


USE HEX KEY PAD TO ENTER DESIRED USER PATTERN. THE RIGHT CURSOR ARROW ADVANCES TO NEXT BYTE POSITION. THE LEFT CURSOR ARROW BACKS UP ONE POSITION.
USER PATTERN
D3 C3 00 00 E6 0D 33 A2 B8
03 E4 22 11 23 44 A1 A4 77
F7 4B FF 89 D3 11 BB 9D 56
13 55 CF AA 88 F3 23 54 65
1F B6 77 FF 00 98 65 D4 5F
22 9A 0D 31 06 06 06 AA 11
44 8B F3 4F 6F D7 8D C9 C0
11 A7 A8 A8 23 01 20 03 44
44 11 09 8D FF FF FF DD 34
56 C1 C2 3C 4C 5C B7 B8 9B
11 34 33 36 0D 00 00 A1 3C
1F 66 77 A7 A8 BB 22 53 62
11 33 5F A2 56 77 C6 9A 92
12 F4 F5 F6 F7 FF 22 11 37
2D AF BF CA 22 34 6C B0 55
15 DOWN
NINE ACROSS
INS
DEL
CLR
INSERT BYTE BY HIGHLIGHTING POSITION FOR INSERTING, THEN DEPRESS INS KEY.
DELETE BYTE BY HIGHLIGHTING POSITION FOR DELETION, THEN DEPRESS DEL KEY
CLEARS ALL USER DATA
NOTE: A MINIMUM OF THREE CHARACTERS MUST BE ENTERED FOR PROPER OPERATION.

LOOPBACK CODES
SET- 21 84 10 42 08 (HEX)
RESET- 49 92 24 (HEX)

Figure 3-12. User Pattern Display

An example of another use is a pattern with a long string of 0's to stress test a regenerative repeater's clock recovery and reshaping capability. Let us assume that the user desires a string of 31 0's. It is necessary to have at least one "1" in the string so the pattern would look like:

10000000 00000000 00000000 00000000 100

HEX 1 HEX 0 HEX 0 HEX 0

The user would enter the pattern in HEX as "10 00" and this would give a 31 zero transmission followed by a 1 and another string of 31 zeroes and so on.

With practice the user can input almost any binary pattern desired. The only restriction being the pattern must be able to repeat within 2048 bytes.

3.4.8 Remote Port Configuration

The REMOTE PORT CONFIG menu, shown in figure 3-10, is located in the upper left hand corner of the matrix of menus. It serves to set up either the serial RS-232 or parallel IEEE-488 ports for control or printer functions.

The data format of the terminal, modem, or printer determines the settings required for serial RS-232 operation. For IEEE-488 parallel interface operation it is only necessary to know the computer's handshake protocol (CR-LF or ACK-NAK) and what address to set the Model 5500 (0-31).

To set up the Model 5500 for operation with a serial printer, follow the steps below:

1. Determine the format of the printer from the operation manual supplied with the device, or use a Phoenix Model 1500 Communications Interface Analyzer to determine the printer settings.

2. Assume, for this example, that the format is CR-LF,1200 baud, 8 data bits, no parity, and 1 stop bit. It is necessary to set the Model 5500 to match this format.

3. The Model 5500 is shipped from the factory with it's RS-232 serial control port configured as a DCE. (Refer to installation section.) This permits direct connection of a terminal or printer. If the internal dip switches have been changed to the "DTE" position for use with a modem then these must be returned to the "DCE" position

4. Using the CURSOR keys, move the half intensity block to the display over the TRACE mode selection.

5. Using the SELECTION key choose either ENABLE or DISABLE. The TRACE mode is normally DISABLED.

6. Use the CURSOR key to move the half intensity block down to PROTOCOL and then use the SELECT key to choose "CR-LF".

7. Repeat this process to select BIT RATE (1200 bps), CHAR. SIZE (8), PARITY (NONE), and STOP BITS (1).

8. Finally, press the soft key opposite the PRINTER block and note that it becomes highlighted.

9. The unit is now ready to print out under command of the PRINT SELECTION menu settings.

10. The REMOTE PORT CONFIG menu offers complete flexibility in the choice of terminals, modems, and printers by allowing the user to adapt to any standard bit rate from 50 bps to 9600 bps; 7 or 8 data bits; odd, even or no parity bits; and 1, 1.5 or 2 stop bits.

Operation of the Model 5500 by a computer or controller over the parallel IEEE-488 bus is identical to operation of the unit over the serial port. The setup of the IEEE-488 port is however, much easier.

The operator need only select the protocol (CR-LF or ACK-NAK) appropriate for the particular computer or controller and then give the unit the address it will be using. Note: CR-LF is the most widely used protocol.

For example the user may have an HP-85 computer or similar IEEE-488 bus controllable device. The Model 5500 can be assigned any address from 0 to 31. Normally a printer and a test set are controlled from one device so the address could be "0" for the 5500 and "1" for the printer. The computer sends out commands to all of the instruments connected to the bus. It prefaces each command to a specific device with the address of that device. All devices connected to the bus "listen" to all the messages on the bus but only react to those which are preceded by their address.

3.4.9 User Stored Program Menu

The purpose of this menu is to enable the user to label (identify) each stored program of test set ups. This feature permits the user to easily recall desired tests that were stored previously.

The USER STORED PROGRAM menu, shown in figure 3-9, is located in the upper right hand corner of the menu matrix.

The user can store the test set ups, parameters, displays, indeed everything needed to test a particular system by pressing the front panel STORE key and then pressing whichever number, 0 to 9, is assigned to that test program.

In order to label the stored program however, the operator must scroll to the USER PROGRAM menu. Labeling cannot be done during the STORE operation.

To label a program once it has been stored, first scroll to the USER PROGRAM menu.

For example, assume that the user has set up the Model 5500's displays for a synchronous 9600 Bps modem test. The test pattern, display parameters, graph, printout parameters and test mode have all been stored as Program 1.

To label Program 1, the operator decides that the data rate and mode will be sufficient to jog his memory.

The Up and Down CURSOR keys are used to move the half intensity block over the 1 in the Program number column. Note that another half intensity block in the program label area moves with the program number block.

Use the left and right CURSOR keys to position the half intensity block in the extreme left side area of the display opposite the number 1.

Next, use the Up and Down SELECT keys to scroll through the character set to the number "9". Then use the Right CURSOR key to move the half intensity block one space to the right. Use the SELECT keys to scroll through the character set up to the decimal point "." Repeat this procedure until the label " 9.6 Kbps, Sync" has been entered.

This procedure requires some patience but has the virtue of not requiring a terminal.

If the user has a terminal, it is suggested that it be used for labeling the program. Use of a printer permits typing and entering the entire label as one item as opposed to entering one character at a time via the keypad.

The procedure for storing and labeling a program over the remote port using the terminal is as follows:

Connect an asynchronous, ASCII terminal, such as a Televideo 912, Wyse 100, or any similar interface async terminal to the RS-232 remote port at the rear panel of the Model 5500. Ensure that the 5500's internal dip switches are set in the "DCE" position so that the terminal can be directly cabled to the model 5500

Next, using the REMOTE CONFIGURATION menu, configure the remote port's data format to match that of the display terminal. For example, assume the terminal operates at the 1200 bps, with an 8 bit character size, no parity bits, and 1 stop bit. Set up the REMOTE CONFIGURATION menu with TRACE disabled, CR-LF protocol, 1200 bps, 8, No, 1 and then press the RS-232 soft key.

Type a "?" on the terminal and press the Return key. If everything is working properly the Model 5500 will download back to the terminal its main "HELP" menu.

Locate the STORE and RECALL commands. Type STORE ? and then press Return. This calls up the HELP menu for the STORE Command.

STORE ? <RETURN>

The Response Will Be:

Form: STORE # -----name-----
Where: # = 0 - 9

The number field selects the memory location into which the current setup is to be stored. The name field is optional. If omitted the present name is retained. The name will be cleared if a null (two single quotes) name is specified. A maximum name length of 16 characters is allowed. Anything past the sixteenth character will be truncated. The STORE command when followed by no parameters returns a ten line response showing program number followed by the assigned name.

Similarly, type RECALL ? and Return to call up the HELP menu for RECALLING stored programs.

RECALL ? <RETURN>

The response will be:

Select program 0 - 9.

To recall a specific program simply replace the question mark in the above example with the number of the desired program. All of the test conditions will be changed to those of the selected program. As with STORE specifying RECALL with no program number will return ten lines showing program number followed by assigned name.

3.4.10 BIG BERT Display

The BIG BERT DISPLAY located to the right of the MAIN BERT DISPLAY is provided as a convenience for the user. This menu allows the selection and display of any two of the twenty seven error measurement parameters which are accumulated by the Model 5500. The BIG BERT menu is a split screen, large format display as shown in figure 3-13.

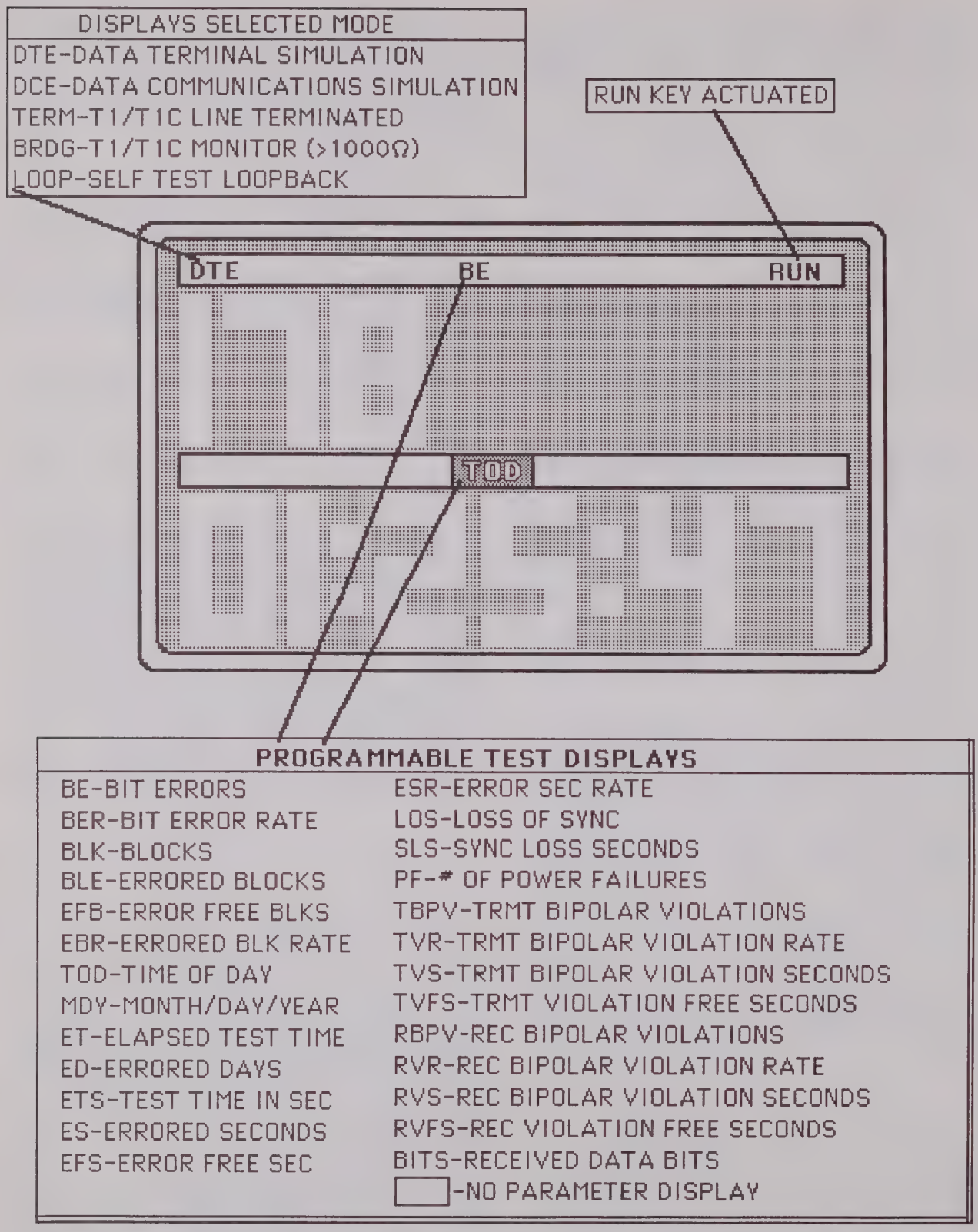


Figure 3-13. Big BERT Display

The user may choose a parameter for display by using the UP/DOWN CURSOR keys to place the half intensity block in the top or bottom half of the display. Then, using the select keys, the user may scroll through any of the parameters being measured and display whichever one is desired.

NOTE: This does not interfere with the test in progress.

The BIG BERT display permits viewing any two from a distance and is helpful when the test technician has to be some distance from the test set.

The test parameters which can be displayed on BIG BERT are any two of the following:

NOTE: Refer to section 4 of this instruction book for definitions and equations which define the following parameters.

BE-BIT ERRORS
ESR-ERROR SEC RATE
BER-BIT ERROR RATE
LOS-LOSS OF SYNC
BLK-BLOCKS
SLS-SYNC LOSS SECONDS
BLE-ERRORED BLOCKS
PF-#OF POWER FAILURES
EFB-ERROR FREE BLKS
TBPV-TRMT BIPOLAR VIOLATIONS
EBR-ERRORED BLK RATE
TVR-TRMT BIPOLAR VIOLATION RATE
TOD-TIME OF DAY
TVS-TRMT BIPOLAR VIOLATION SECONDS
MDY-MONTH/DAY/YEAR
TVFS-TRMT VIOLATION FREE SECONDS
ET-ELAPSED TEST TIME
RBPV-REC BIPOLAR VIOLATIONS
ED-ERRORED DAYS
RVR-REC BIPOLAR VIOLATION RATE
ETS-TEST TIME IN SEC
RVS-REC BIPOLAR VIOLATION SECONDS
ES-ERRORED SECONDS
RVFS-REC VIOLATION FREE SECONDS
EFS-ERROR FREE SEC
ALRM-INDICATES YELLOW ALARM(B,2)
BITS-RECEIVED DATA BITS
SIGNALING FRAME BIT ERRORS(S)
LOSS OF PCM(C)
TERMINAL FRAME BIT ERRORS(F).

NOTE: Bipolar Violation data and Alarm status indications are only available with certain Interface Module options.

3.4.11 Other Menus

The optional displays are discussed in the options section of this instruction book.

3.5 ACTIVITY INDICATORS

There are 12 green LED's on the 5500 front panel to indicate activity of the installed interface module.

The actual points being monitored are on the TTL interface between the module and control board. Since there are many different module options, all front panel indicators may not be applicable to a particular interface.

In addition, some of the indicators change meaning when modes are switched between DTE and DCE.

Tables 3-3 and 3-4 relate the LED's to the interface circuit being monitored, for each module and mode of operation.

The LED indicators provide interface activity status as well as mode (RUN), async, sync recovery and error injection status. These provide a quick visual indication of what is occurring at the interface and can often lead to rapidly identifying the source of a problem. For instance, if the Model 5500 is transmitting data and the TD LED is lit but there is no received data (RD LED not lit) then it is possible that the transmission source at the distant end is not functioning. This could be a modem which is receiving data but whose transmit section has become defective.

Table 3-3. RS-232/RS-449 Activity Indicators

INDICATOR	ACTIVITY			
	RS-232		RS-449	
	DTE	DCE	DTE	DCE
TD/RD	Xmit Data	Rx Data	Send Data	Recount Data
RD/TD	Rx Data	Xmit Data	Receive Data	Send Data
RC/RC	Rx Clock	Rx Clock	Rec. Timing	Rec. Timing
TC/TC	Tx Clock	Tx Clock	Xmit Timing	Xmit Timing
RTS/DCD	Rqst to Send	5500 Data Carrier Det.	Rqst to Send	Rec. Ready
CTS/RTS	Clear to Send	Clear to Send	Clear to Send	Rqst to Send
DSR/DTR	DSR	DTR	Data Mode	Terminal Rdy
DTR/DSR	DTR	DSR	Terminal Rdy	Data Mode
DCD/CTS	Data Carrier Det.	Clear to Send	Receiver Rdy	Clear to Send
RI/RI	Ring Ind	Ring Ind	Incoming Call	Incoming Call
SQ/SQ	Signal Qual	Signal Qual	Signal Qual	Signal Qual
SCTE/SCTE	SCTE	SCTE	Terminal Tim	Terminal Tim

Table 3-4. T1/T1C and V.35 Activity Indicators

INDICATOR	ACTIVITY			
	T1/T1C	FRAMED T1	V.35	
			DTE	DCE
TD/RD	Transmit Data	Transmit Data	Transmit Data	Receive Data
RD/TD	Receive Data	Receive Data	Receive Data	Transmit Data
RC/RC	Recovered Receive Clock	Gated Internal Clock	Element Timing Xmit Signal	Element Timing Xmit Signal
TC/TC	Recovered Xmit Clock	Gated Internal Clock	Element Timing	Element Timing Data Channel Rec
RTS/DCD	X *	X *	Request to Send	Line Signal Det
CTS/RTS	X	N/A	Ready for Sending	Request to Send
DSR/DTR	X	X	Data Set Ready	Data Terminal Ready
DTR/DSR	X *	X	Data Terminal Ready	Data Set Ready
DCD/CTS	X	X *	Receive Data Channel Receive Line Signal Detector	Drive Ready for Sending
RI/RI	X	X	Calling Indicator	Calling Indicator
SQ/SQ	X	X	X	X
SCTE/SCTE	Internal Clock Source	Gated Recovery Receive Clock	Transmitter Signal Element Timing (DTE Source)	Transmitter Signal Element Timing (DTE Source)

* May be control signals pertinent to internal 5500 functions on these monitored lines.

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5500
Data Communications
Analyzer

Phoenix
microsystems

Phoenix Instruction Book

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application

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4.1 GENERAL

Bit Error Rate Testing, whether at 75 bps rates or 1.544 Mbps rates, has a common purpose in digital circuit maintenance. That purpose is to determine whether or not a given transmission path can support a digital transmission without errors.

To test a digital circuit and determine whether or not errors are being generated it is customary to employ a test set which generates a known pattern and transmits it over the circuit. The circuit may be "looped" at the distant end or another test set may be located there. In any event, the pattern received is compared bit by bit to the known pattern generated and any discrepancies in the received pattern are counted as errors.

Since a known pattern must be substituted for the live traffic in order to perform a Bit Error test, these tests are often referred to as "out of service" tests.

The test patterns employed are pseudo-random or user sequences of binary digits which simulate live traffic. The term "pseudo-random" implies that the stream of bits only appears to be random. While the test pattern bit stream must appear to be random to simulate live traffic, it still must have some repetition in order for the test set to detect and recover the pattern.

Other patterns beside pseudo-random sequences are useful for test purposes, and not necessarily for Bit Error Testing. The Model 5500 provides a pattern generator capable of generating pseudo-random sequences of length 63 bits, 511 bits, 2047 bits, Reversed 2047 bits, (2^15)-1 bits, (2^20)-1 bits, and the Quasi-Random Word which is a (2^20)-1 bit long pattern with greater than 14 zero suppression. In addition, the Model 5500 pattern generator is capable of generating All Marks, All Spaces, Alternate Mark/Space, T1 CSU Set Code, T1 CSU Reset Code, FOX message, and USER input patterns of up to 135 characters in HEX.

The variety of digital equipments to be tested, both DCE and DTE, is so vast that the choice of pattern depends upon a number of factors. For example a pseudo-random sequence 63 bits long is fine for a low speed modem testing. At 300 baud or even 1200 baud the 63 pattern looks like regular traffic. However, if we attempted to use this pattern at higher data rates (T-1 for example) then the "random-like" nature of this pattern would disappear. It is also possible that certain pseudo- random sequences may generate long strings of zeros. Some systems have real problems with long strings of zeros. In particular, T-1 carrier systems operating at 1.544 Mbps, restrict data patterns to no more than 14 consecutive zeros.

As a rule of thumb, the choice of patterns follows the bit rate of the device or system under test. The higher the bit rate the longer the pattern and vice versa. Thus we see 511 patterns used for testing 1200 baud modems and the QRW used to test T-carrier systems.

No test set, no mater how good it is, can substitute for the experience of the operator when it comes to resolving a problem in the transmission path. All the test set can do is provide the tool for analyzing the symptoms of the problem and, if possible, increase the diagnostic ability of the technician by providing him with accurate information.

The Model 5500 increases the diagnostic ability of the user by measuring and displaying up to twenty-seven error parameters plus bias distortion, frequency, event, time, and optional jitter simultaneously. The Model 5500 places all of the analysis tools in one instrument and provides all of the test results simultaneously. This improves the user's ability to solve problems faster because the Model 5500 can simulate the problems (inject errors or jitter) and analyze the symptoms simultaneously to point the finger in the right direction as fast as possible.

To aid the user in making the most use of the Model 5500, the following section details and defines the various Bit Error Rate Testing parameters.

4.2 BERT DISPLAY OPTION DEFINITIONS

The definitions of the BERT parameters are provided to promote an understanding of what is being measured and how it is being measured.

ALRM - ALARMS:

This parameter provides the user with information on the status of the receive side of the system under test and is available with the Model 5500-624 Framed T-1 Interface Option. Since there is not much point in trying to run a bit error test on a system in an alarm condition until the alarm has been cleared, this parameter can be very useful. In fact, four alarm states are displayed on this block. The first alarm state is B2. This is the so-called YELLOW ALARM. It means that bit number 2 in each of the twenty four received PCM channels making up to the T-Carrier were forced to 0 for more than 50 milliseconds. This indicates that the terminal equipment at the remote end of the circuit has lost synchronization or that there has been no incoming DS-1 for more than two seconds. The T-Carrier format is an interleaved pattern of twelve bit lengths. Six of these bits are signaling frame bits (S-bits) while the other six bits are terminal frame bits (F-bits). The second alarm state is indicated by an S. S signalling bit errors are detected when a sequence of 5 S-bits contains four consecutive ones (01111). Once set the alarm continues until three consecutive "zero" bits are preceded and followed by a "one" S-bit (10001). The third state, loss of PCM, is indicated by a C on the ALRM display block. If a string of 31 or more consecutive zeros is received, or if no data transitions occur for 2 or more seconds, the C indication is displayed. The fourth state is indicated by an F on the ALRM display. This indicates that an F-bit is received which is not the inverse of the last F-bit and the same condition also occured two, three, or four F-bit frames earlier. The presence of one or more of these four characters on the ALRM display indicates an abnormal condition which must be investigated and cleared before continuing with any error testing. The normal indication on the ALRM display is an all dots pattern (.....,). The four states occupy the following positions (B2.S.C.F.), and any one or all could be present at one time. Note that these are qualitative and not quantitative indications. It is more important to know that these conditions exist than it is to count how often they occur.

BE - Bit Errors:

The known generated pattern is compared, by the detector, to the received pattern on a bit by bit basis. Any received bit which does not agree with what is known to have been sent is counted as an error. The error data is accumulated in a 16 bit register which is accessed by the processor every 1 millisecond. No error occurrences can be left undetected to a probability of 1^{-16}.

BER - Bit Error Rate:

The Model 5500 is capable of providing the user with two bit error rates. One is a continuous bit error rate which changes as the number of bits received increases. This provides the user with a running indication of the "health" of the circuit under test at all times rather than forcing the user to set in a number of bits, wait for the unit to process the data, calculate a BER number for the test length, and wait to be restarted to measure BER again. The user can, of course, force the Model 5500 to emulate other test sets by choosing a combination of block length and number of blocks in test to yield a specific bit length test. For example assume that the user desires to have the Model 5500 compute BER for a test length of 10^5 bits, Choose a block length of 10^3 bits/block and 100 blocks for the number of blocks to be tested and you have a total of 10^5 bits. Press RUN and at the end of the 10^5 bits the Model 5500 will stop. At that time the BER block will have a numerical result which is the BER for the 10^5 BITS. Of course the user could obtain 10^5 bits by using a 10^4 block size and 10 blocks to test or a 10^5 block size and 1 block to test.

The Bit Error Rate is calculated based upon the bit errors and number of bits received. The Model 5500 is capable of providing this calculation on an on-going basis or a one time basis. The advantage of the running bit error rate is that it allows the user to track the ups and downs as the test progresses rather than have to wait until the end of the test to get an answer.

$$BER = \frac{\text{Bit Errors}}{\text{Number of Bits Received}}$$

The BER is updated at least once per second while testing is underway since this is the minimum update rate of the CRT.

BITS - RECEIVED DATA BITS:

This parameter is presented in scientific notation as, for example, 3.9^6 which means 3.9 million bits have been received.

BLE - ERRORED BLOCKS:

This is the number of blocks received with at least one bit in error. A block error will be counted whether one error or fifty errors occurs during the block.

BLK - BLOCKS:

This is the number of blocks received by the Model 5500. This number steadily accumulates during a test and is composed of all blocks both errored and error free. Setting the block length on the Model 5500 (10^2 to 10^9) determines what the receiver looks for and calls a block. The Model 5500 will start to count when it is running and has acquired sync.

ED - ELAPSED DAYS:

The length of the test in days. Partial days are measured by the 'ET' parameter.

EFB - ERROR FREE BLOCKS:

This is the number of blocks received without an error in them and is calculated as:

BLOCKS - ERRORED BLOCKS = ERRORED FREE BLOCKS.

EFS - ERROR FREE SECONDS:

This important parameter is often used to characterize a data link. It is defined as the number of seconds during which no errors have occurred. It is counted by the Model 5500 when the unit is running and has acquired sync. The total of ES plus EFS is equal to the ETS.

ES - ERRORED SECONDS:

This parameter is one of the more important measurement results. An error second is said to have occurred if at least one error occurs in the one second interval. The model 5500 measures "synchronous" errored seconds (a bit error event initiates the errored second timer). Errored seconds, like all measurements, will start to be accumulated by the Model 5500 when it has begun to RUN and it has acquired sync.

ESR - ERRORED SECONDS RATE:

This is the number of errored seconds divided by the number of seconds.

ESR = ES/ETS = ES/(ES+EFS)

This parameter can easily yield other qualitative results for the user. In particular, the user can derive the % of Errored Seconds and % of Error Free Seconds quite easily from ESR. To obtain the percent errored seconds simply multiply the numerical result in the ESR display window by 100. For example, assume the reading for ESR is 3.1 E-2. Multiplying 3.1 x 102 by 100 yields the result 3.1% Errored Seconds. The percent error free seconds can be easily calculated by subtracting the 3.1% from 100% which yields 96.9% error free seconds.

ET - ELAPSED TIME:

This is the elapsed test time in hours/minutes/seconds since the RUN/STOP switch was set to RUN and the Model 5500 acquired sync. Elapsed time will not accumulate if the unit is not in sync or during sync losses. This counter operates in a 24 hour mode with rollovers accumulated in ED.

ETS - ELAPSED TIME IN SECONDS:

This is the elapsed test time given in total seconds as opposed to the hours/minutes/seconds given by ET.

LOS - LOSS OF SYNC:

This parameter is based upon a bit error rate threshold being crossed. That is, when the bit error rate becomes excessively high, the Model 5500 will at some point, declare that it has lost sync and will not recover sync until the bit error rate drops below the threshold. The sync loss threshold in the Model 5500 is adjustable. It is factory set for initiating a sync loss whenever any 1000 bits received contains 100 or more errors. That is a BER 10-1 or higher. When the Model 5500 is out of sync, error parameter collection is meaningless and therefore only the time the unit is out of sync is accumulated.

In order to change the sync loss threshold it is necessary to remove the top cover from the Model 5500. Remove the two Phillips head screws in the rear top cover retaining rail and slide the cover out the back. Located above the CRT on the main control board between IC's U20 and U35 is a 14 pin header with jumper straps on it. (Refer to figure A) The jumper straps control the sync loss criteria as described below.

SYNC LOSS CRITERIA

1. X, Y, and Z must be high.

2. 1, 2, 4, 8, 16, 32, 128, 256, and 512 are the outputs of the bit error counter.

3. Patch the bit error outputs to X, Y, and Z as desired to select a count/thousand bits. Only one output at a time may be patched to X, Y, or Z.

4. EXAMPLE 1: (as shipped from factory)
   X to 64 (pin 1 strapped to pin 11)
   Y to 32 (pin 2 strapped to pin 10)
   Z to 4 (pin 3 strapped to pin 7)
   X+Y+Z=1 64+32+4 = 100 errors/thousand bits or BER = 10^{-1}

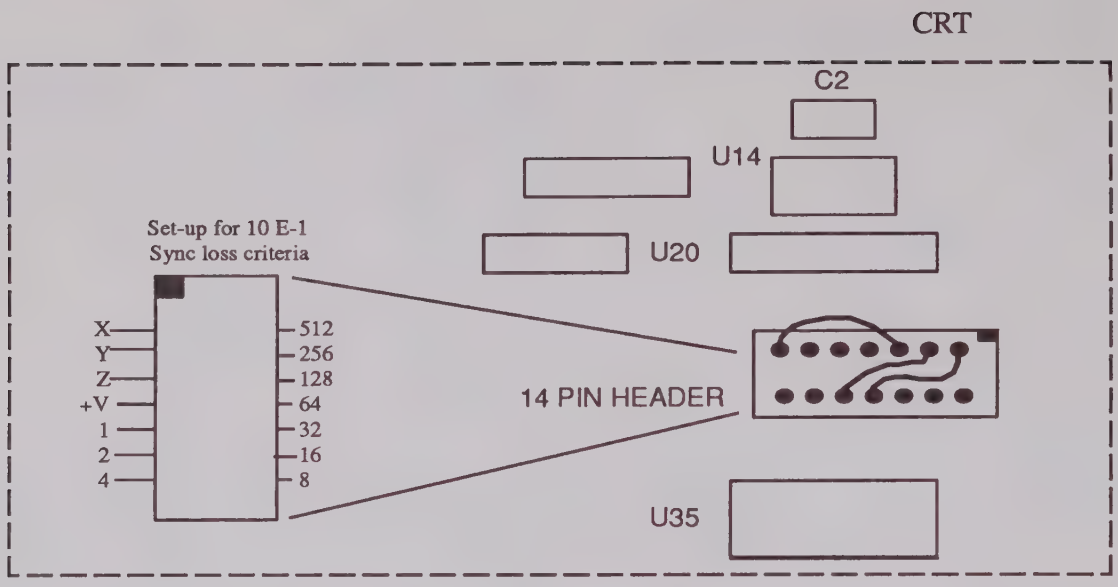


Figure A. Sync Loss Threshold 14-Pin Header

5. EXAMPLE 2:
   X = 128 (pin 1 strapped to pin 12)
   Y = 64 (pin 2 strapped to pin 11)
   Z = 8 (pin 3 strapped to pin 8)
   X+Y+Z = 64+32+8 = 200 errors/thousand bits or BER = $2x10^{-1}$

6. EXAMPLE 3:
   X = 1 (pin 1 strapped to pin 5)
   Y = +V (pin 2 strapped to pin 4)
   Z = +V (pin 3 strapped to pin 4)
   X+Y+Z = 1+0+0 = 1 error/1000 bits.

This connection sets the minimum BER threshold for a sync loss at 1x10-3.

The sync loss threshold can be varied from 8.96x10-1 errors/bit to 1x10-3 errors/bit. A loss of sync is also counted if data transitions do not occur for more than two seconds.

MDY - MONTH/DAY/YEAR:

The month, day, year are available to date stamp any events printed out. The setting is retained in non-volatile memory. The settings are changed like any other parameters from the BERT FORMAT menu.

PF - POWER FAILURES:

The Model 5500 will count power failures to its input power supply. The threshold for counting a power failure is 90 Volts AC (180) Volts AC if operating from 1 220-240 VAC source). or less. The enables the operator to determine whether or not AC power was continuously available during long term unattended tests. Note that upon powering up the Model 5500, a power failure will be indicated (if in the RUN mode) so the user should always press the CLEAR "soft key" at the lower right of the main BERT CRT display before doing any testing.

NOTE: The following error parameters are applicable to the T- Carrier interface module options such as the Model 5500- 600 and 5500-624.

RBPV - RECEIVE BIPOLAR VIOLATIONS:

These are bipolar violations of the AMI line code which occur on the receive pair. Unlike the TBPV parameter, BPV's on the receive side of the line can be measured when the Model 5500 is operating in the TERMINATED mode as well as the BRIDGE mode.

RVFS - RECEIVE VIOLATION FREE SECONDS:

The count of the number of seconds on which no violations occurred on the receive pair of the T-Carrier under test.

RVR - RECEIVE VIOLATION RATE:

The rate at which receive BPV's occur. The RVR parameter can be measured in both the BRIDGED and TERMINATED modes. It is calculated as:

$$\text{RVR (violations/bit)} = \frac{\text{RBPV}}{\text{number of bits}}$$

RVS - RECEIVE VIOLATION SECONDS:

This is a count of each second in which at least one receive violation occurs.

SLS - SYNC LOSS SECONDS:

This represents the total accumulated time the unit is out of sync. A single sync loss of very short duration (much less than 1 second) will not cause the SLS counter to record. The sync loss itself will be counted but a sync loss second is not necessarily counted. The counter will, however, accumulate the outage time so that, for example, if each sync loss had a duration of 200 milliseconds then after 5 such occurrences the counter would increment and display a 1 in the SLS block. It is important to note that the information is not lost but only waiting for the total outage to reach 1 second.

TBPV - TRANSMIT BIPOLAR VIOLATIONS:

This parameter is the count of violations of the Alternate Mark Inversion (AMI) bipolar line code format used for T1 and T1C transmission in the U.S. In this case, the BPV's are being monitored on the transmit pair of four wire T-Carrier system, hence the designation TBPV. This parameter is only measured by the Model 5500-600 module option operating in the Bridge Mode. In this mode this interface option has two receivers active and can monitor both the transmit pair and the receive pair of a full duplex T-Carrier. Transmit line bipolar violations, TBPV, may be measured in the BRIDGE mode, or may be injected at a programmed rate (but not measured) in the TERMINATE mode when the Model 5500 transmitter is enabled.

TOD - TIME OF DAY:

The time of day in hours, minutes, and second is available to time stamp any events printed out. The setting is retained in non-volatile memory.

TVFS - TRANSMIT VIOLATION FREE SECONDS:

The number of seconds without a bipolar violation. The sum of TVS and TVFS equals the elapsed time in seconds (ETS).

TVR - TRANSMIT VIOLATION RATE:

The rate at which transmit BPV's occur. The TVR parameter can be measured only in the BRIDGED mode. It is calculated as:

$$\text{TVR (violations/bit)} = \frac{\text{TBPV}}{\text{number of bits}}$$

TVS - TRANSMIT VIOLATION SECONDS:

This is a count of each second in which at least one bipolar violation occurs. It is similar in usage to errored seconds (ES).

4.3 BERT FORMAT AND TEST DEFINITIONS

The following terms located on the BERT FORMAT menu and certain test measurements from the main BERT menu are defined in detail to assist the operator in making maximum use of the 5500 test set capabilities Refer to figure 3-5 for a typical BERT FORMAT menu display.

TOD - TIME OF DAY:

This is the time of day in hours/minutes/seconds plus day of the week and month/day/year. Once the user has set in the correct times this information is retained in non-volatile memory.

CLOCK INV - CLOCK INVERT:

The user may invert the polarity of the Transmit, Receive, or External Clock Signals. The half intensity block is placed over the clock signal to be inverted and then the SELECT keys are used to choose normal or inverted operation. When inverted, an "I" is displayed by the parameters as for example "IRC" which denotes that the Receive Clock signal is inverted. Any or all of the clock signals may be inverted if desired or all may be left in normal mode.

DATA INVERT - DATA INVERT:

This display block allows the user to invert the transmit or receive data or both independently. This is accomplished in the same manner as Clock Inversion but is independent of that parameter. The user may for example choose to let the Transmit Clock, send Transmit Data out inverted and Receive Data in normal polarity.

BIT RATE - BIT RATE:

The next selection on the FORMAT menu is the bit rate. This parameter can also be selected from the main BERT menu. If a numerical bit rate such as 75,..., 19.2k,..., 1.544M is chosen, then the Model 5500 will supply the clock to the system under test. However, when testing synchronous modems it is normal to have the modem supply the clock. In this case, the Model 5500 should be set to EXT for bit rate and then the test set will use the clock on the receive clock pins to time the transmit data output. The internal bit rates which can be selected arelisted in figure 3-5. The OPT CLK choice refers to the optional precision clock for specific frequency which the user may choose to purchase. The USER CLK choice refers to the rear panel clock input on the Model 5500. The user may input a frequency synthesizer to the USER CLK BNC connector and select any frequency from 75 bps to 13 Mbps for operation.

MODE - MODE:

The Model 5500 is capable of synchronous or asynchronous operation. Generally speaking, most systems operating at 2400 baud and above are synchronous with the exception of certain compressed bit rate voice systems. The Model 5500 can operate at bit rates up to 48 Kbps asynchronously.

DCE SYN TD CLK - DCE MODE SYNCHRONOUS TRANSMIT DATA CLOCK:

When the user selects DCE simulation operation of the Model 5500 it is necessary to then select whether the test set (simulating a MODEM) will supply clock (TC-Pin 15) to, or derive clock (XC-Pin 24) from the system under test in synchronous operation. If the user selects TC then the Model 5500 Transmitter's clock source is its own internal clock. If XC is chosen then the Model 5500 Transmitter derives its timing from the system under test. Note that this selection is only meaningful in synchronous DCE mode simulation and is primarily used only when operating at speeds greater than 1 Mhz.

CHAR SIZE - CHARACTER SIZE:

The number of data bits which make up a character in asynchronous data transmission is selectable from either the FORMAT or main BERT menus. Asynchronous character sizes of 5, 6, 7, or 8 bits length may be chosen. If CONTINUOUS is chosen then the Model 5500 sends out a continuous stream of data bits without start and stop characters. When operating in a synchronous mode there are no start and stop bits and so the bit stream is continuous or infinite.

PARITY - PARITY: Parity bits in the data stream provide a means of error detection. In async data streams the user may select EVEN or ODD parity or may choose NO parity at all. Choosing EVEN parity means that the number of 1's in a data block must add up to an even number. Likewise ODD parity means the number of 1's in the block of data sums up to an odd number.

If, in EVEN parity, a block is received with three 1's in it, then the detector knows there has been at least one error. The choice of parity or no parity depends entirely on the system under test.

STOP BITS - STOP BITS:

Asynchronous, Byte oriented data transmissions employ start and stop bits to identify one byte from the next. A typical data transmission may be composed of a start bit, seven data bits, a parity bit and a stop bit. The choice of STOP BITS is either 1 or 2 and depends upon the system under test's data format. This parameter has no meaning in synchronous transmission, and is not displayed in that mode.

PATTERN - PATTERN:

The choice of pattern depends upon the test which the user desires to make. The Model 5500 uses industry standard pseudo-random sequences of various lengths for Bit Error Rate testing plus a number of other patterns for specific uses as well as a USER programmable pattern up to 135 HEX characters long.

BLOCK SIZE - BLOCK SIZE:

The number of bits which make up a block can be varied from 100 (10^2) to 1,000,000,000 (10^9). The choice of block size is a factor in the overall test length in bits since the block size times the number of blocks on the test equals a specific number of bits. The choice of block size may be dictated by any number of factors but in general the higher the bit rate the longer the block size.

BLOCKS - BLOCKS:

The number of blocks in the test may be selected as any number from 1 to 9999. If a '0' is placed in this window then the Model 5500 will run a test continuously until the STOP key is pressed. The user selects the BLOCKS by moving the half intensity marker to BLOCKS and setting in the desired number using the HEX keypad numbers. This parameter may also be changed from the main BERT menu.

INJ ERROR RATE - INJECT ERROR RATE:

The Model 5500 enables the user to inject single or multiple bit errors at rates from 9^{-3} to 1^{-9} errors/bit. The soft key labeled INJ on the main BERT menu controls the injection of errors. Momentarily pressing the INJ soft key on and off injects single errors. Pressing the INJ key on and leaving it on causes errors to be injected at whatever rate the user has set the INJECT ERROR RATE to. The user programs the error rate by scrolling the half intensity block over the INJ ERROR RATE field. The user must select the mantissa of the rate desired using either the SELECT keys or the HEX keypad. The choices are 0 to 9. A '0' will disable the error inject. Then the user must use the CURSOR key to move the block to the right and change the exponent from -3 to -9 as desired.

Note: The SELECT keys may also be used to scroll the inject rate up and down. In this mode scrolling past '9' up or '0' down automatically adjusts the exponent as well. This allows the error rate to be smoothly scrolled to a threshold for testing of error correction/detection equipment.

Once set, the rate is retained in non-volatile memory. Error Injection is most often used for identification and testing the integrity of a circuit.

TIMER START - TIMER START:

The Model 5500 can measure the time delay between any two of the primary interface signal occurrences when RS-232, V.35 or RS-449 Interface Module options are used. The Model 5500 can measure time between occurrences up to 4.67 minutes in duration. The measurement resolution varies with the scale select from 1 microsecond to 10 milliseconds. The START selection is the signal which will initiate the time measurement as for example, RTS/" or RTS rising edge.

TIMER STOP - TIMER STOP:

This selects the event which will stop the event timer. For example, if the timer was initiated by "RTS/" then the stop signal may be "CTS /". The time delay between the next occurrences of these two events is displayed on the main BERT menu.

AUTO RESYNC - AUTO RESYNC:

This function normally enables the auto sync loss recovery. The user would normally leave this in the ENABLE position. However, some specialized requirements may require that this function be disabled. In this case the unit never "sees" a sync loss and will continue counting and testing regardless of error rate. This is selected by choosing DISABLE. Caution is advised in the use of this function.

LOOP - LOOP:

The LOOP function is part of the Model 5500 self testing capability. By selecting LOOP with the soft key to the right of the CRT, the user causes the interface module to loop back its transmit and receive data and clocks. This provides a convenient means of checking out the operation of the Model 5500.

Note: During normal testing conditions LOOP should not be operating.

4.3.1 Interface Option Definitions

Items which are unique to the T-Carrier Interface Module options such as the Model 5500-600, -624, -700, -800 series are defined in the Options section of this instruction book.

4.4 BER TEST ASSISTANCE

Table 4-1 presents a list of possible problem areas if the Model 5500 does not achieve synchronization with the device under test.

4.5 USER PATTERN GENERATION

The user pattern allows the user to construct a pattern for transmission by the Model 5500. Selecting the USER pattern causes the Model 5500 to transmit a repetitive pattern of whatever the operator has placed in the USER PATTERN display. The user is permitted to enter up to 135 characters in HEX from the front panel HEX keypad or from a printer over the Remote Control ports. Each character in HEX is an 8 bit long word so the total bit length which could be input is 1080 bits. However, the user may enter as few as three characters if desired.

NOTE: If the RAM retention battery becomes discharged or is replaced the Model 5500 will power up default to the system configuration menu and will flash fail at the user pattern block. This "error" can be ignored or the user may choose to place three or four characters into the User Pattern display. These can be any HEX characters the user may want to place in memory. Refer to section 3.4.7 of this instruction book for more detail on USER PATTERN function.

4.6 GRAPH DISPLAY MODE FOR BER TESTING

The GRAPH DISPLAY located at the left of the MAIN BERT DISPLAY in the menu matrix provides the user with an important tool in locating the source of a problem.

Often, the cause of a burst of errors may be related to its time occurrence. That is, a large air conditioner or other high power device may cycle on and the surge may cause a nearby terminal or modem to suffer a power line hit. The events can be correlated to the cause using the GRAPH DISPLAY.

The operator may choose to plot up to four different error parameters versus time so as to generate a more complete picture of what and when is going on in a circuit.

A typical graph display of bit errors is shown in figure 3-7. A typical test set up might involve graphing bit errors, sync losses, bipolar violations (T-Carrier testing), and errored blocks. Other parameters can be graphed but generally speaking, the above are the most important in isolating problems. The set up of the GRAPH display is described in detail in section 3.3.3.

The graph display stores up to sixty hours of data in up to one minute intervals if only one parameter is graphed. This permits long term unattended testing (over a weekend for example) without losing the data, or when it occurred.

Table 4-1. BER Test Assistance

PROBLEM	CORRECTIVE ACTION
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Check bit rates, sync/async mode, character size, parity etc. Verify that correct mode (DCE or DTE) has been selected. Verify that correct mode (RTS/DCD) has been selected. Verify that CLOCK and DATA inverts (BERT format menu) are properly selected. Verify that BRIDGE mode in T-Carrier testing has not been selected. (BRIDGE mode disables the Model 5500 transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units. Also, in SYNC mode, ensure that one unit supplies clock and the other is set to EXT clock.

Table 4-1. BER Test Assistance (Cont)

PROBLEM	CORRECTIVE ACTION
SYNC LED blinks on and off in synchronous testing	If two test sets are operating in an end to end test verify that one is set to supply clock (internal timing) and the other is set to EXTERNAL clock. If a modem or other device in the circuit is the master clock, set both sets to external. Note: There can be only one Master Clock in a synchronous circuit.
SYNC LED not illuminated and TD LED is off	Verify that RTS is activated if unit is configured as DTE.
Constant bursts of errors detected in testing synchronous devices	Select External clock mode if not already selected. (Most synchronous devices are strapped to supply clock).
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.
Test suddenly stops and RUN LED goes off	If continuous testing is desired verify that '0' has been placed in the Number of Blocks test window and press RUN. If testing a specific number of blocks verify that the number of blocks selected has been reached when test set stops. This is normal operation.
Model 5500 displays errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. Note that T1 carrier systems are only specified to provide a 1^{-6} error/bit rate which is about three errors or less every two seconds.
RAM error on power-up	Battery may be discharged. Leave power on unit for 24 hours to fully charge battery.

When setting up a GRAPH DISPLAY for a long term test it is suggested to set the HORIZONTAL time scale to sixty minutes per division and the VERTICAL scale to x1 for the maximum sensitivity. This will cause even single events to be displayed. When the user wishes to view the display the scales can always be changed for a more convenient display. No data is lost by changing the scales.

The user also can print out the graphic data (for a single parameter). The Model 5500 will print out data continuously in 1, 10, or 60 minute increments depending upon the horizontal scale setting and the user can therefore bypass the 60 hour limitation of the GRAPH DISPLAY itself.

Figure 3-6 details the setup for graph data (BERT PRINT MENU). Figure 3-7 details the actual graph display and display controls. Table 4-3 presents the graph definitions. The Model 5500 graph is provided only under local control. For remote control, an intelligent controller may be used to obtain data plots.

4.7 FREQUENCY MEASUREMENT

The Model 5500 is also a frequency counter with a resolution of 0.1 HZ below 1 MHZ and 1 HZ above 1 MHZ. The reading is displayed on the main BERT menu as shown in figure 3-3. The user may select BR to view the Asynchronous Baud Rate, or TC (Transmit Clock), RC (Receive Clock) or XC (External Clock) in synchronous system testing.

The Model 5500 counter provides the user with a reasonably accurate diagnostic tool for uncovering frequency related error problems. This enables the user to spot a drifting clock. When the test set is set up in the EXT Clock mode, the user can measure and determine the stability of the Receive Clock by selecting RC. When acting as a synchronous DTE it is convenient to check the outgoing clock by selecting TC. The user can easily compare the Transmit and Receive clocks for significant differences. When a USER clock input to the rear panel BNC connector has been selected the user can measure it on the TC of Transmit Clock field.

The user may measure the external clock (Pin 24 on the RS-232 interface module) signal by selecting XC. This would be used when the Model 5500 is deriving its clock from an external source such as a modem or terminal to time its transmitter.

Frequency counter display accuracy is a function of the stability of the internal 4.608 MHZ reference clock oscillator. The Model 5500 uses a software controlled correction to zero out the impact of the crystals in accuracy and so all that remains is the effect of thermal stability or drift. This is typically less than 5 parts per million with the standard crystal and can be reduced to 1 part per million or less with the precision clock (Model 5500-CL01) option.

The software controlled calibration command for the frequency counter - TWEAK - is described in detail in section 4.10-REMOTE PROGRAMMING.

4.8 EVENT TIMING

The Model 5500 measures the time interval between transitions of any two selected interface signals to 4.67 minutes duration with a resolution of 1 microsecond to 10 milliseconds depending upon scale.

RTS /	DTR /
RTS \	DTR \
RD /	DCD /
RD \	DCD \
TD /	DSR /
TD \	DSR \
SQ /	CTS \
SQ /	CTS \

The "/" character after a signal indicates that signal going "TRUE". For an RS-232 interface, a MARK to SPACE (1 to 0) Transition is the TRUE condition. The "\" character shows a transition to FALSE. On a TTL interface a "HIGH" to "LOW" transition is the TRUE condition. If an 'I' is displayed after the reading at least one event has occured but the event is inactive now. A '-' display indicates the selected event has not occurred. The user selects the resolution as 1US, 10US, 100US, 1MS, or 10MS, and then chooses which two events are to be measured. The Model 5500 automatically measures the time delay between the transitions, and updates the measurements display on a continuous basis.

4.9 BIAS DISTORTION (SKEW)

The Model 5500 measures BIAS DISTORTION on the receive data lines. A pattern having a uniform 50/50 distribution of 1's and 0's is customarily used as the transmitted signal. Any of the Model 5500 pseudo-random sequences may be used.

Bias is determined as the time ratio of MARKS (1's) to MARKS + SPACES (0's) and expressed as a percentage.

A reading of 0% indicates a constant SPACE signal while a reading of 100% indicates a constant MARK signal. A 50% reading indicates ideal symmetry of MARK bit widths periods to SPACE bit widths periods.

A reading of 45% to 55% is considered acceptable in most systems. Some older modems may have larger windows of acceptable performance but in general readings outside the 45-55% range maybe cause for further investigation.

Table 4-2. Graph Definitions

SYMBOL	DEFINITION
Crsr 1	The main cursor for the graph used to determine the exact time and magnitude of the data being plotted. The UP SELECT key advances the cursor in the time increments set by the horizontal resolution. The DOWN SELECT key backs up the cursor in time. A time of day clock reading is provided next to the Crsr 1 display.
Crsr 2	Cursor 2 is used for the plot printing function. Data between Cursor 1 and Cursor 2 can be printed out by depressing the SOFTKEY corresponding to 1-2 in the PRINT SELECTION menu.
Horizontal (Horiz)	CRT field that displays the time scale selected. One, ten or sixty minutes per division may be selected. Thirty time divisions can be displayed without scrolling to the right. The resolution decreases as the number of parameters to be graphed increases.
Vertical (Vert)	CRT field that displays the vertical scale factor. Factors from 1 to 100,000 are provided.
Mag 1	Displays the magnitude of the data at Cursor 1 position.
Mag 2	Displays the magnitude of the data at Cursor 2 position.
ALL	Softkey used to print entire sixty hour graph plot. Will also enable continuous printout of graph data.
1-2	Prints graph data between Cursor1 and 2 only.
DAT	Softkey used to select numerical data print out instead of graphic data. Used with any standard Rs-232 interface printer.
GRAPH DATA	CRT field used to select data parameter(s) to be plotted.

If a modem or other device has filters shaping the bit stream, and they have degraded band pass characteristics which favor 1's over 0's or vice versa then the likelihood of an error occurring is increased.

Bias Distortion was more of a problem with older FSK type modems employing lumped element filters than it is with modern modems which use digital filter techniques.

Bias Distortion measurement accuracy is +1%, and the reading is updated at least once per second.

4.10 REMOTE PROGRAMMING

The Model 5500 provides either an IEEE-488, or RS-232 remote control port. This allows its test functions to be controlled, and results recorded from a terminal, a modem link, or a computer. Complete unattended remote testing may be performed.

4.10.1 Initial Set Up and Operation

Refer to figure 3-9 for detailed set up options for the RS-232 or IEEE 488 ports. Selection of the "IEEE 488

t", or "RS-232 t" trace mode enables the user to view the characters being sent to and from the Model 5500 over these ports on the CRT line with "] [" showing.

Front panel controls may be used while the remote port is in operation unless specifically locked out with the "LOCK" command.

4.10.2 Remote Interface Protocol

The Model 5500 operates using the 7 bit ASCII code. Commands to the Model 5500 consist of strings of ASCII characters in the range from space (20H) to DEL (7FH) terminated by a carriage return (ODH). Characters less than 20H are ignored except for back space (08H) which functions as a delete.

The response from the Model 5500 can take on one of several formats depending upon the selected protocol.

1) IEEE-488/CRLF

In this mode, commands which result in the Model 5500 sending a response expect it to be formatted as follows:

Char 1
"
"
Char x
CR
LF EOI

The controlling device should be set to terminate its input on either the line feed character code or the assertion of the EOI line.

2) IEEE-488/ACK

Unlike the previous mode, in which the controller operated in an open loop manner, the ack protocol provides a response to each command regardless of whether the command returns data. If the command is understood an ACK (06H) character is returned. If an error is encountered in interpreting the command, NAK (15H) is returned. If additional data is to be returned it follows the first ACK and is terminated by a second ACK. The three possible responses are shown below.

(error) NAK EOI

(good, no data) ACK EOI

(good, data) ACK
char 1
"
"
char x
ACK EOI

NOTE: In all cases the EOI line indicates end of response.

3) RS232/ACK

Operation of the RS-232/ACK protocol is identical to the IEEE-488 protocol with the exception that there is no EOI line. It is the controllers responsibility to know whether or not additional data is expected following the first ACK. In practice this knowledge comes naturally with the program organization.

This protocol uses a half duplex data transfer structure on the RS232 port. The Model 5500 controls data flow to itself through the DTR line and sends data via the RTS/CTS handshake.

4) RS232/CRLF

This mode is intended primarily for use with a directly connected terminal. It operates full duplex and echos every character received. In this mode DEL and Back Space send a character sequence, the response to which will delete the last character. A control-x will cause the Model 5500 to ignore the present line. If an error is encountered in interpreting the input line it is reprinted to the error point and a '?' is inserted. The response to commands is shown on the line following the command.

4.10.3 Command Description

Commands to the Model 5500 are divided into two basic types. The first command type is used to configure the test setup. Commands of the second type are used to read test results.

Configuration commands have three formats. The first format is the command issued by itself (for example 'BR' for Bit Rate). When issued with no parameters, all of the configuration commands return their present setting. A second format is to follow the command with '?' in the parameter field (for example 'BR ?' for all possible Bit Rate settings). In response to this format the 5500 returns either a list of all possible settings for this command or a description of the parameter setting format. The final format is the command followed by a valid parameter. This results in the immediate update of the selected function to the specified state (for example 'BR 9600' sets the Bit Rate to 9600 Bps).

The second command type is used to read test results. These commands ignore any data past the command field and always return the present value of the selected function. In most cases, the value returned in response to

one of these commands is a snap-shot of the parameters value at the instant the command is evaluated. The exceptions to this are event time, frequency measurement and bias. These three measurements are configured such that repeated requests will result in a newly measured value for each response. This allows for the gathering of meaningful data in cases where statistical analysis will be done on the readings. Note: this can result in response delays of up to 10 seconds when reading event times and approximately 1 second when reading either frequency or bias.

In addition to the the two command types described above, certain commands are dependent upon the type of interface. At the present these are divided into commands which function with all interface modules, those which function only with the T1/T1C interface and those which function with any interface other than T1/T1C. In the following tables which define the various commands this is noted with an (A) for all, (T) for T1/T1C only and (NT) for other than T1/T1C.

4.10.3.1 Test Set Up Commands Table 4-3 presents the test set up commands and their definitions.

4.10.3.2 Test Results Commands Many of the test result variables consist of counters which accumulate as the test is run. Except where noted otherwise below, all of these counters can accumulate up to 9,861,472 before overflowing. When this value is reached the counters wrap to 0. The read value will have 'OVF' appended to it if overflow has occurred.

A second variable type is associated with rate calculations (Bit Error Rate, Block Error Rate, Errored Second Rate, etc.). These variables are calculated from two of the counter variable types described above (for example: Block Error Rate = errored blocks/total blocks). Overflow of either of the counter variables which are used to calculate the rate variable results in the rate variable also being returned with the 'OVF' tag appended. The rate variable calculations have a dynamic range from 1.00^{-0} to 9.99^{-99}. The cleared state for these variables is 0. All rate calculations are carried to 4 digits with the displayed result 4/5 rounded to 3 significant digits. As with all other variables readable from the Model 5500, the rate variables are calculated "on-the-fly" and represent the rate at the instant the command is evaluated.

As in the previous table the commands presented in table 4-4 are tagged with an (A) if they are valid with all interfaces, a (T) if they are valid with the T1/T1C interface only, or (NT) if they are valid with interfaces other than T1/T1C

4.10.3.3 Miscellaneous Commands The commands presented in table 4-5 do not fit in either of the two basic command types described above. They provide general system control and status as well as additional help features to the user.

4.10.4 Remote Port Pin Assignments.

4.10.4.1 RS-232 Port Pin Assignments

PIN	FUNCTION	SOURCE
3	RD	USER
2	TD	5500
5	CTS	USER
4	RTS	5500
20	DTR	5500
8	DCD	USER

4.10.4.2 IEEE-488 Port Pin Assignments

PIN	FUNCTION
1	D101
2	D102
3	D103
4	D104
5	E10
6	DAV
7	RFD
8	DAC
9	IFC
10	SRQ
11	ATN
12	CHASSIS
13	DIOS
14	D106
15	D107
16	D108
17	REN
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND

Table 4-3. Test Set Up Command Definitions

CMD	DEFINITION
BLKS	Selects the number of blocks to test end. The allowed range of values is from 0 to 9999. When 0 is selected, testing is continuous with no automatic end of test. (A)
BPVRATE	Selects bipolar violation inject rate. Rates from 9E-3 to 1E-7 are selectable. If the mantissa is set to 0, BPV injection is disabled. Also see 'INJ'. Options: The injected BPV rate is programmable in the form: mE-e Where: m = 0,1,2,3,4,5,6,7,8,9 is the mantissa e = 3,4,5,6,7 is the exponent. (T)
BR	Selects the transmit and receive bit rate. Forty two internally generated rates from 50 bps to 3.152 Mbps are available as well as USER, EXTERNAL, and Optional clock selects. Options: USER, 0, 75, 110, 134.5,150, 300, 600, 1200, 1800, 2400, 4800, 7200, 9600, 14.4K, 16K, 19.2K, 32K, 48K, 56K, 57.6K, 64K, 72K, 76.8K, 112K, 115.2K, 128K, 153.6K, 168K,192K, 224K, 230.4K, 256K, 384K, 448K, 460.8K, 512K,672K, 768K, 1.024M 1.344M, 1.544M, 3.152M, EXTERNAL (NT)
BS	Selects the number of bits per block from 100 to 1 billion. Options: 10^2, 10^3, 10^4, 10^5, 10^6,10^7, 10^8, 10^9 (A)
CS	Async character size may be set from 5 to 8 bits or continuous (clock recovery mode). Options: 5, 6, 7, 8, CONT (NT)
DISPLAY	Selects the displayed front panel menu. Options: BERT, FORMAT, PROG, PAT, PRINT, CONFIG, GRAPH, GPRINT, REMOTE, BLACK, BIG (A)

Table 4-3. Test Set Up Command Definitions (Cont)

CMD	DEFINITION
DTR/DSR	Sets DTR 'true' or 'false' (DSR in the DCE simulation mode). Options: Either "T" for TRUE of "F" for FALSE (NT)
ESTART	Selects the start condition for the event timer. Options: RD/, RD\, RI/, RI\, SQ/, SQ\, DTR/, DTR\, DCD/, DCD\, DSR/, DSR\, CTS/, CTS\, RTS/, RTS\ (NT)
ESTOP	Selects the stop condition for the event timer. Options: RD/, RD\, RI/, RI\, SQ/, SQ\, DTR/, DTR\, DCD/, DCD\, DSR/, DSR\, CTS/, CTS\, RTS/, RTS\ (NT)
FSRC	Selects the clocking signal to be measured. Options: BR, TC, RC, XC (A)
INJ	Master enable/disable for logic error and/or bipolar violation injection. Note: Logic and BPV injection can be individually disabled by the 'IRATE' and 'BPVRATE' commands. Options: OFF, ON (A)
IRATE	Selects the logic error inject rate from 9E-3 to 1E-9. If mantissa is set to 0 logic error injection is disabled. Also see 'INJ'. Options: The injected error rate is programable in the form: mE-e Where: m = 0,1,2,3,4,5,6,7,8,9 e = 3,4,5,6,7,8,9 (A)

Table 4-3. Test Set Up Command Definitions (Cont)

CMD	DEFINITION
LOCK	Disables front panel control of the specified function. Options: ALL, RUN/STOP, INJECT, CLEAR,SYNC, RTS/CTS, DTR/DSR, DCE/DTE, RECALL, STORE, SELECT **(A)**
LOOP	Selects internal loop around of transmit data to receive data. This provides a selftest of the 5500's transmitter and receiver. Options: OFF, ON **(A)**
MD	Sets the Model 5500 to SYNC or ASYNC mode. Options: ASYNC, SYNC **(NT)**
PAT	Selects the test pattern to be used. Options: 63, 511, 2047, 2047 REV (2^15)-1, (2^20)-1, QRW, T1SET, T1RESET, MARK, SPACE, ALT, FOX, USER **(A)**
PR	Selects parity in async mode. Options: NONE, EVEN, ODD **(NT)**

Table 4-3. Test Set Up Command Definitions (Cont)

CMD	DEFINITION
RECALL	Recall Model 5500 user program 0 to 9. Options: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 **(NT)**
RTS/CTS	Sets RTS 'true' or 'false' (CTS in DCE simulation mode). Options: Either "T" for TRUE of "F" for FALSE **(NT)**
SB	Selects number of stop bits in async mode. Options: 1, 2 **(NT)**
SIM	Selects simulation of DCE or DTE interface. Options: DTE, DCE **(NT)**
STORE	Stores the present setup into the selected user program. Options: The format to store a program is: STORE x 'program name' Where: x = program number (0 to 9) **(NT)**

Table 4-3. Test Set Up Command Definitions (Cont)

CMD	DEFINITION
SYNC	Controls and displays the receiver sync status. Options: Either "R" to reset sync loss or "B"to force sync break. Responses: BRK - searching for sync, not yet acquired. SYNC - in sync, no sync loss. LOSS - has been in sync, is now out of sync and searching to reacquire. RCOV - in sync, sync has been lost and was reacquired. **(A)**
TCODE	T1/T1C data stream coding format. Selection is both hardware and software selected. Options: AMI, B8ZS or HDB3, B6ZS **(T)**
TOD	Time-Of-Day clock. The TOD clock operates in a 24 hour mode. To set: TOD hh:mm Seconds are zeroed when clock is set. Read back format is: hh:mm:ss.t Where: hh = hours (0 to 23) mm = minutes (0 to 59) ss = seconds (0 to 59) t = tenths of seconds (0 to 9) **(A)**

Table 4-3. Test Set Up Command Definitions (Cont)

CMD	DEFINITION
TMODE	Select T1/T1C interface termination mode. Termination may be either 100 ohms (terminated) or 1000 ohms (bridge). Options: BRIDGE, TERM Note: Use BRIDGE mode when monitoring T1/T1C data stream. (T)
TWEAK	Model 5500 frequency measurement calibration. This variable is set to the actual frequency of the 5500's 4.608 Mhz reference clock. The value must be between 4.606 Mhz and 4.61 Mhz. This value is stored in nonvolatile RAM. It is checked on power up to assure it is in the proper range. If the read value is outside of the set range, the nominal value of 4.608 Mhz is used. Calibration can be verified by comparing the measured 4.608 Mhz frequency to the stored tweak value. (A)
UNLOCK	Unlocks all or selected front panel function selects. Options: ALL, RUN/STOP, INJECT, CLEAR, SYNC, RTS/CTS, DTR/DSR, DCE/DTE, RECALL, STORE, SELECT (A)
USRPAT	Sets the user pattern. The user pattern may be up to 135 characters in length and must be a minimum length of 3 characters. Options: Enter HEX data separated by spaces. Enter '+' before the data to add it to the present pattern. Otherwise, the old pattern is replaced by the new data. Example 1: USRPAT 01 02 03 04 sets the user pattern to: 01,02,03,04

Table 4-3. Test Set Up Command Definitions (Cont)

CMD	DEFINITION
USRPAT	Example 2: USRPAT + 08 10 20 40 80 if it followed the previous example would result in the user pattern: 01,02,04,08,10,20,40,80 **(A)**

Table 4-4. Test Results Command Definitions

CMD	DEFINITION
BA	Blocks Analyzed. This response is the number of blocks analyzed. See 'BS' above from description of block size. **(A)**
BE	Bit Errors. Responds with the number of bit (logic) errors which have occurred. **(A)**
BER	Bit Error Rate. Calculated as follows: BER = BE/BITS Where: BE = bit errors BITS = Total Bits analyzed **(A)**
BIAS	Bias. Mark to Space ratio. Calculated as the percentage of the 1 second sample period spent in the Mark condition. **(NT)**
BITS	Bits analyzed. The source of this variable is dependent upon the termination mode of the T1/T1C interface. In the Bridge mode this variable is the product of the data rate (T1=1.544 Mbps, T1C=3.152 Mbps) and the elapsed time (ET). In the Terminate mode Bits is the product of blocks analyzed (BA) and block size (BS). **(T)**
BLE	Block Errors. This response is the number of blocks with at least one bit error. **(A)**
EBR	Errored Block Rate. This is the rate at which errored blocks occurred. It is calculated as: EBR = BLE/BA Where: BLE = number of errored blocks BA = number of blocks analyzed **(A)**

Table 4-4. Test Results Command Definitions (Cont)

CMD	DEFINITION
EFB	Error Free Blocks. This response is the number of blocks with no bit errors. **(A)**
EFS	Error Free Seconds. This response is the number of seconds in which no bit errors occurred. **(A)**
ES	Errored Seconds. This response is the number of seconds in which at least one error occurred. **(A)**
ESR	Errored Second Rate. This response is the rate at which errored seconds occurred. It is calculated as follows: ESR = ES/ETS Where: ES = number of errored seconds ETS = elapsed test time in seconds **(A)**
ET	Elapsed Test Time. This is a running clock of the total in-sync test time. It is formatted as follows: hh:mm:ss.t Where: hh = hours (0 to 23) mm = minutes (0 to 59) ss = seconds (0 to 59) t = tenths of seconds (0 to 9) Note: only in-sync seconds are accumulated. See 'SLS' for out of sync time accumulation. **(A)**
ETS	Elapsed Test Time in Seconds. Similar to 'ET' above except response is in seconds (0 to 9,861,472 seconds) **(A)**
EVENT selected	Event Time. This response is the time between the start and stop events selected by 'ESTART' and 'ESTOP' above. The event time measurement is returned in seconds with a maximum resolution of 1 ns and a maximum value of 4.75 seconds. If the event has not occurred the response will be '-'. If the event is greater than 4.75 seconds the response will be 'OVF'. If more than 10 seconds have elapsed since the last event time measurement was made the response will have an 'I' appended to it indicating inactivity. **(NT)**
LOSS	Sync Losses. This response is the number of times sync loss has occurred. **(A)**
MFREQ	Measured Frequency. This response is the frequency of the line selected by the 'FSRC' command. The range of measurement is from approximately 150hz to 16mhz. Resolution is .1hz from 150hz to 1mhz and 1hz from 1mhz to 16mhz. No clock or a clock > 150hz results in a response of 'UNDER' indicating under range. Clocks > 16mhz result in a response of 'OVER' indicating over range. **(A)**

Table 4-4. Test Results Command Definitions (Cont)

CMD	DEFINITION
RBPV	Receiver Bipolar Violations. This response indicates the number of bipolar violations which have occurred on the receive data line. **(T)**
RVFS	Receiver Bipolar Violation Free Seconds. This response indicates the number of seconds in which no bipolar violations were detected on the receive data line. **(T)**
RVR	Receiver Bipolar Violation Rate. This response indicates the rate at which bipolar violations occurred. It is calculated as follows: RVR = RBPV/BITS Where: RBPV = receiver bipolar violations BITS = total bits **(T)**
RVS	Receiver Bipolar Violation Seconds. This response indicates the number of seconds in which one or more bipolar violations were detected on the receive data line. **(T)**
SLS	Sync Loss Seconds. This response is the total elapsed time in which the Model 5500 was out of sync with the incoming data stream. NOTE: This time is internally accumulated with a resolution of 1msec. For this reason it is possible to accumulate several sync losses before registering the first sync loss second. **(A)**
TBPV	Transmitter Bipolar Violations. This response indicates the number of bipolar violations detected on the transmit data line. NOTE: This variable is only available when operating in the Bridge mode. **(T)**
TVFS	Transmitter Bipolar Violation Free Seconds. This response indicates the number of seconds in which no bipolar violations were detected on the transmit data line. NOTE: This variable is only available when operating in the Bridge mode. **(T)**
TVR	Transmitter Bipolar Violation Rate. This response indicates the rate at which bipolar violations occurred. It is calculated as follows: TVR = TBPV/BITS Where: TBPV = transmit bipolar violations BITS = total bits NOTE: This variable is only available when operating in the Bridge mode. **(T)**
TVS	Transmitter Bipolar Violation Seconds. This response indicates the number of seconds in which one or more bipolar violations were detected on the transmit data line. Note: This variable is only available when operating in the Bridge mode. **(T)**

Table 4-5. Miscellaneous Command Definitions

CMD	DEFINITION
?	System Help Menu. This command returns a list of all system command words and a brief command description.
RUN	Start test. If test is already in progress this command is ignored.
R/S	Run/Stop status. This command responds with the present test status. Options: RUNNING, STOPPED
STATUS	System Status. This command returns the status of the various system self tests which are performed on power up. Either 'PASS' or 'FAIL' will be indicated for the static and dynamic RAM tests as well as the ROM, user program and user pattern checksum tests.
STOP	Stop test. If test is already stopped this command is ignored.
TRATE	T1/T1C interface module rate. The T1/T1C interface module operating speed is set by two dip switches on the module. This command returns the present setting of these switches. NOTE: if the switches are not set to a valid state this command returns '???'. Options: T1, T1C, ???
VER	Software Version Level. This command returns both the model and software version number of the unit. A typical response would be: Phoenix 5500, Vers. 2.02

4.11 TWEAK PROCEDURE

The following procedure should be followed when making the **TWEAK** adjustment as described in table 4-3.

1.Place the 5500 power switch to the "OFF" position.

2. Remove the top cover of the 5500 by removing the two top cover screws at the rear of the unit.

3. Place the 5500 power switch to the "ON" position.

4.Connect the terminal to 5500 remote port with an RS-232C cable.

5. Press the **RECALL** switch on the 5500 front panel.

6. Press 2 on the front panel keypad (to select the remote configuration menu).

7. Press the **GO TO** softkey to activate the remote configuration menu.

8. Use the remote configuration menu to match the 5500 to the terminal in use. Select RS-232 and CR-LF.

9. Connect a frequency counter to pin 15 of U87 (refer to figure B below).

NOTE: Use a HP Model 5315B (with option 4) frequency counter or equivalent. (Option 4 is a temperature compensated crystal for increased accuracy.)

10. Connect the frequency counter ground to signal ground test point as shown in figure B.

11. Type **TWEAK (space) XXXXXXX** (where xxxxxxx = seven (7) digits displayed on the frequency counter.)

12. The zero offset in the frequency reading has now been removed from the frequency counter in the 5500.

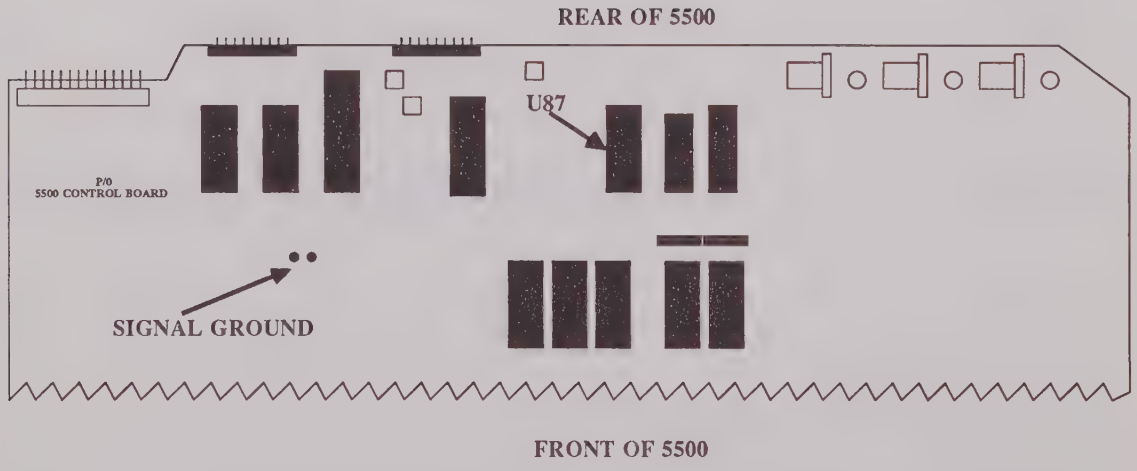


Figure B. TWEAK Adjustment Locations on 5500 Control Card

application note #1

Testing a T-1 Link

1.0 INTRODUCTION

High-speed, T-carrier facilities are gaining momentum. T-carrier systems are those that conform to a series of standards established by AT&T for the formatting of data for transmission at high speeds. These systems include multiplexing equipment, channel service units (CSUs), channel banks, transcoders, and others. This application note covers testing of one of the T-carrier systems, the T-1.

T-1 is the first T-carrier being implemented on a wide scale. T-1 circuits are 1.544Mbps trunk circuits that can be used for voice, data, and video transmission. To transmit an analog voice channel, T-1 equipment digitizes a PAM pulse stream using 8-bit PCM encoding. The PAM samples produce a transmission rate of 64Kbps for each digitized voice channel, compatible with many digital PBXs on the market today.

T-1 testing has become a hot topic for the simple reason companies need to increase their bandwidth capabilities. And communications alternative technologies are often the most cost-effective means of transporting data at very high speeds.

1.1 PURPOSE

The purpose of this application note is to describe typical T-1 testing and the use of the Phoenix Model 5500 Data Communications Analyzer in performing the analysis.

On portions of T-1 circuits implemented using radio, coax, lightwave, or satellite, the data travels as modulation on a carrier frequency. The figures of merit most often used to judge the performance of T-1 circuits include bit error rate (BER) and error free seconds (EFS). At the termination of the T-1 links and on portions of T-1 circuits implemented on T-1 span lines, the signal is transmitted as a digital bipolar waveform. A binary "1" is transmitted as a positive or negative polarity pulse while a "0" (zero) is represented by the absence of a pulse. Each successive "1" is transmitted at the opposite polarity of the one preceeding. This coding rule is called alternate mark inversion (AMI). Bit error analysis is one of the methods used to measure the transmission performance of T-1 lines. In addition to error analysis, the pulse alternation property of bipolar transmission provides a means for testing the lines while in service. This method is refered to as bipolar violation analysis. A bipolar violation occurs whenever the noise and distortion on a span line is high enough to cause a pulse to be missed when it was transmitted or to be detected when no pulse was present. This results in two successive pulses of the same polarity, thus violating the AMI code. Receive bipolar violation rate (RVR) and receive bipolar violation free seconds (RVFS) are the usual measurements which may be performed without interrupting service on the T-1 link.

Digital repeaters are installed on the T1 span line at 6000 foot intervals to regenerate the digital signal. At these regeneration points, the 1544Khz timing signal is stripped off, or recovered, from the bipolar signal. To ensure that this clock is recovered, the bipolar signal must change states before clock signal is lost. AMI-coded signals are restricted to no more than 15 consecutive zeros. Another coding scheme, expected to come into wider use in the future is B8ZS. The Bipolar with 8 Zero Substitution code transmitts a code containing intentional bipolar violations in place of each string of eight consecutive zeros.

T1 data streams are transmitted in both framed and unframed formats. Most private microwave radio link is not required to have framing information. However, all T1 circuits passing through AT&T facilities must contain framing information. The Phoenix 5500 used with the Model 5500-624 Interface Module, provides all the capabilities for total T1 link testing with either D4 framed or unframed data.

NOTE: The Model 5500-624 interface module may also be equipped with the J02 option to allow the testing of T1 lines for high speed jitter in accordance with AT&T specifications.

2.0 T1 LINE TESTING

2.1 BIT ERROR TESTING

The Phoenix Model 5500 is connected as shown in figure 2-1 for bit error analysis of a T1 line. The Phoenix 5500 replaces the T1 multiplexer and/or terminal equipment on one end of the link and the far end is looped back toward the originating end. In this configuration the originating end must operate on a T1 signal with the combined timing jitter of both the transmit and receive paths. If the jitter is excessive it may create link synchronization problems and prohibit loopback testing. In this case full duplex testing should be performed using a second 5500 at the far end.

The 5500 is generally connected to the T1 line through a channel service unit (CSU). The Phoenix 1544 CSU, shown in figure 2-1, provides the proper termination for the T1 circuits, regenerates the T1 signal, and provides remote loopback capability.

The 5500 sends out a T1 SET code to cause the far end CSU to loopback for testing. The 5500 will automatically switch from T1 SET to QRW a few seconds after testing begins. This is to prevent the T1 SET code from being looped back to the near end CSU causing the near end CSU to go into the loopback mode. If the near end CSU goes into the loopback mode, it would remove the 5500 from the test loop. Upon completion of the test, the user should send T1 RESET code to the far end to take the far end CSU out of the loopback mode.

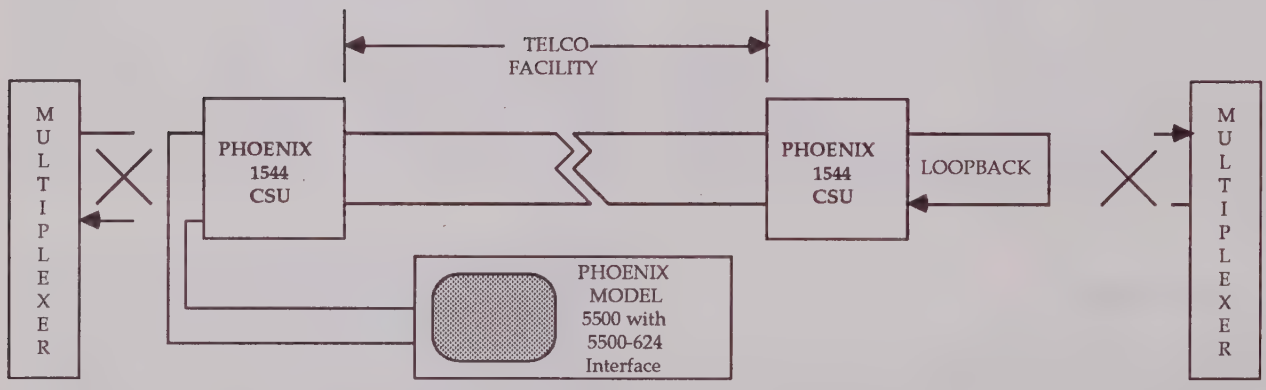


Figure 2-1. T1 BIT Error Testing with Phoenix 5500

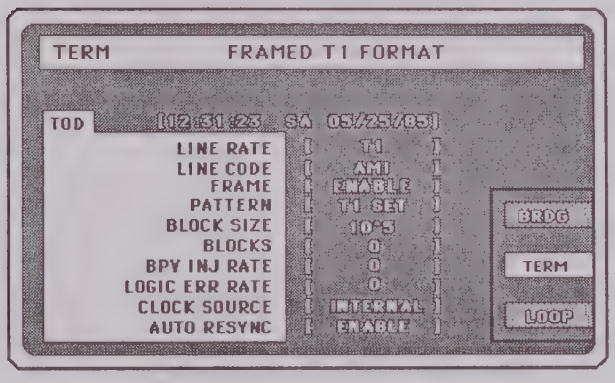
2.1.1 Equipment Required

1 Phoenix Model 5500 Data Communications Analyzer
1 Phoenix Model 5500-624 Interface Module

2.1.2 Equipment Setup

Before applying power to the Model 5500, install the 5500-624 Interface Module. Connect the equipment as shown in figure 2-1.

Turn on the 5500. Depress the **RECALL** switch one time. This will bring the HELP menu to the screen. Enter 6 from the front panel keypad and then press the **GOTO** SoftKey. The FRAMED T1 FORMAT screen should appear as shown below:



Setup the 5500 using this screen as follows:

IMPEDANCE: Using the SoftKey select **TERM**. The **BRDG** (Bridge) position is selected when the 5500 is used as a receive only monitor, and is connected across a terminated T1 line. (Note: Always use the "Bridge" position when connecting the 5500 to a monitor jack.)

TOD: Use the **CURSOR** keys to move the cursor over TOD (Time of Day). Use the **CURSOR** keys to move the cursor over the units in the TOD field. Use the HEX keypad to enter the appropriate alpha/numeric value into the selected parameter.

LINE CODE: Use the **CURSOR** keys to move the cursor over LINE CODE. Use the **SELECT** keys to set the line code to AMI as shown above.

FRAME/UNFRAMED: Use the **CURSOR** keys to move the cursor over FRAME. Use the **SELECT** keys to select ENABLE or DISABLE. For circuits passing through AT&T facilities, select ENABLE. Either ENABLE or DISABLE may be selected for other circuits, depending on circuit requirements.

PATTERN: Use the **CURSOR** keys to move the cursor over PATTERN. Use the **SELECT** keys to set the pattern to T1 SET. This pattern sends out the standard T1 CSU loopback code to cause the remote CSU to loopback for test purposes. After the 5500 begins the test it will revert to QRW. QRW (quasi-random word) is a (2^20)-1 pseudo-random sequence which employs >14 zero suppression and is the prefered pattern for T1 tests.

BLOCK SIZE: Use the **CURSOR** keys to move the cursor over BLOCK SIZE. Use the **SELECT** keys to set the BLOCK SIZE (a 100K block size is recommended for a T1 link test).

BLOCKS: Use the **CURSOR** keys to move the cursor over BLOCKS. Use the **SELECT** keys to set the number of BLOCKS for the test. Normal BER testing of a T1 link requires a minimum of 10^{11} bits be analyzed before printing the final results. At normal error rates, this will require about 18 hours of testing. Selecting "0" permits continous testing.

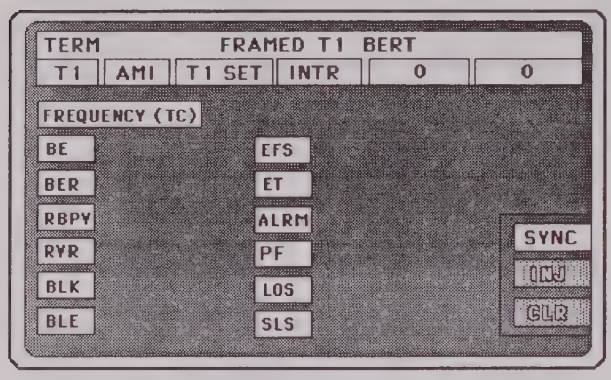
BPV INJ RATE: Use the **CURSOR** keys to move the cursor over BPV INJ RATE. Use the **SELECT** keys to set the BPV INJ RATE to 0. This disables the error inject circuitry which will not be used for BIT Error testing.

LOGIC ERR (INJECT) RATE: Use the **CURSOR** keys to move the cursor over LOGIC ERR RATE. Use the **SELECT** keys to set the LOGIC ERR RATE to 0. The logic errors are what TELCOs call bit errors to distinguish them from BPV errors. Logic errors will not be injected when BIT Error testing is in progress.

CLOCK SOURCE: Use the **CURSOR** keys to move the cursor over CLOCK SOURCE. Use the **SELECT** keys to select INTERNAL. This permits the 5500 to act as the master clock on the T1 line. INTERNAL is always selected when doing loopback testing.

AUTO RESYNC: Use the **CURSOR** keys to move the cursor over AUTO RESYNC. Use the **SELECT** keys to select ENABLE which will allow the 5500 to automatically resynchronize after a synchronization loss.

Press the **MENU** down key one time to select the FRAMED T1 BERT menu as shown below:



This menu will be used to complete the setup of the 5500 for the T1 bit error testing by selecting the parameters the user desires to view during the test. The user may select any 12 of the following parameters for display:

BE = bit errors
BER = bit error rate
BLK = blocks
BLE = errored blocks
EFB = error free blks
TOD= time of day
ET = elapsed test time
ETS = test time in sec
EFS = error free seconds
ESR = error second rate
BITS = recv'd data bits
RVR = Rec BPV rate
RVS = Rec BPV seconds
RVFS = Rec BPV free seconds
LOS = loss of sync
SLS = sync loss seconds
PF = # of power failures
RBPV = rec. BPV'S
EBR = errored blk rate
MDY =month/day/year
ED = errored days
ES = errored seconds
☐ = No parameter display

ALRM = Indicates yellow alarm (B2), signaling frame bit errors (S), loss of PCM (C), and frame bit errors (F). An all dots pattern indicates normal operation on a D4 framed span.

NOTE: Section 4.2 of this instruction book provides full definition of the above parameters.

NOTE: The following choices of parameters for display are for the purpose of demonstrating how to setup the 5500. The operator is free to select any parameters of interest. Also, parameters may be changed at any time during the test without effect on the test being run.

Use the **CURSOR** key to move the cursor over the top left parameter field. Use the **SELECT** key to scroll the parameter list until BE is present. The known generated pattern is compared, bit by bit. Any received bit which does not agree with what is known to have been sent is counted as an error. The error data is accumulated and displayed in this field.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter list until BER appears in the field. This field will now provide a running indication of the health of the circuit under test.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until RBPV appears in the field. This field will provide a count of the receive side bipolar violations.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until RVR appears in the field. This field will keep track of the receive violation rate.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until BLK appears in the field. This field will keep track of the number of blocks received during the test and is composed of all blocks, both errored and error free.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until BLE appears in the field. This field will keep track of the number of blocks received which had at least one bit in error.

Use the **CURSOR** key to move the cursor one position to the right and 5 positions up so that the cursor is on the top right field. Use the **SELECT** key to scroll the parameter field until EFS appears in the field. This field will now indicate the total error free seconds since the start of the test. This parameter is often used as a measure of quality for a T1 line.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until ET appears in the field. This field will then record in hours/minutes/seconds the time since the RUN/STOP switch was set to run and sync was acquired. (ET does not accumulate when the 5500 is not in sync or during sync losses.)

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until ALRM appears in the field.This field will display the alarm staus of the receive side of the circuit. A bit error test on a

circuit with alarms will yield false/invalid results. This field will allow the operator to maintain a watch on the circuit for alarms. (See section 4.2 of this instruction book for a detailed explanation of the ALRM parameter.)

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until PF appears in the field. This field will then record the number of power failures that occur at the 5500 power input during the test.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until LOS appears in the field. This field will keep track of the number of times the bit error rate threshold has been crossed. (Refer to section 4.2 of this instruction book for detailed information on bit error rate threshold.)

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until SLS appears in the field. This field will accumulate the total time the 5500 is out of SYNC.

The setup of the 5500 to perform bit error testing on the T1 data link is now complete.

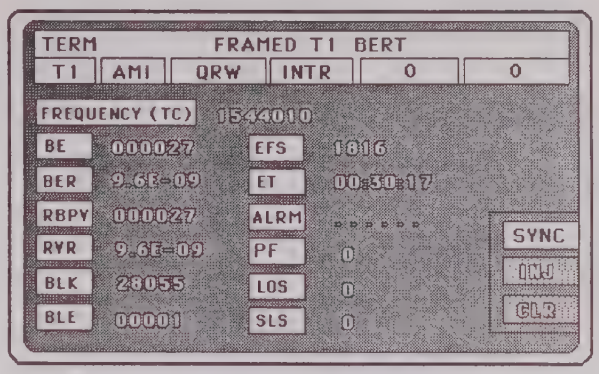
2.1.3 Test Performance

Ensure that the Model 5500 is connected to the near end CSU as shown in figure 2-1. Press the **CLR** softkey to set all the internal counters in the 5500 to zero. Press the **RUN/STOP** switch on the front panel of the 5500. If the remote CSU is appropriately equipped (it will be if it is a Phoenix Model 1544) it will detect the T1 SET code and automatically begin looping data back to the near end. If the far end CSU does not have the automatic loopback feature, a manual patch will have to be made on the far end. Upon successful loopback the 5500 should gain synchronization and begin error analysis. This is indicated by the illumination of the SYNC led on the front panel.

If the SYNC led does not illuminate, recheck all connections and switch settings. (Refer to table 3-2 on (T1) Page 9 in the options section of this instruction book.)

2.1.4 Test Result Evaluation

After the 5500 has obtained sync and begins to collect test data, the operator need only observe the front panel CRT display to begin his analysis of the T1 circuit under test. The display might appear as shown below:



From the above display the following information can be obtained.

The test is presently running (RUN is displayed in upper right cornor of display) and the 5500 is in sync (SYNC is indicated on right side of screen opposite softkeys). The T1 SET code has been replaced by the QRW code (second line from the top, between AMI and INTR). The frequency of the internal clock (transmit) is 1.544010MHz.

The test has been running for 30 minutes and 17 seconds (ET parameter).

There have been 1816 error free seconds (EFS parameter) out of a total of 1817 seconds ((30 minutes x 60) + 17).

There have been 27 bit errors (BE parameter) for a bit error rate of 9.6E-09 (BER parameter) and 27 receive bipolar violations (RBPV parameter) for a receive bipolar violation rate of 9.6E-09 (RVR parameter).

During the test time we have received 28,055 blocks (BLK parameter) and one block has had at least one error (BLE parameter).

The power has not failed (PF parameter), there are no alarms (ALRM parameter), and we have not lost sync (LOS and SLS parameters).

AT&T's performance objective is to provide T1 service at 95% error free seconds measured over any 24 hour period. Such a circuit should exhibit a bit error rate less than 10^{-6} when measured over the same time period.

2.2 BIPOLAR VIOLATION MONITORING

Figure 2-2 depicts the proper method to connect the Phoenix 5500 to monitor bipolar violations on a T1 line. In this configuration, the 5500 is connected across the T1 line while live traffic is being transmitted. The 5500 is connected across the line by using the receive monitor jack on the 1544 CSU (most CSU's provide this feature).

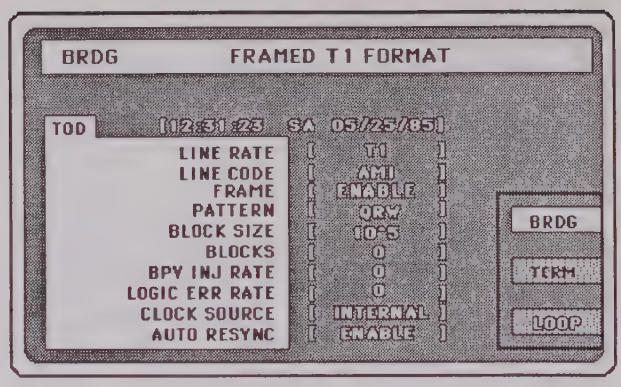
2.2.1 Equipment Required

1 Phoenix Model 5500 Data Communications Analyzer
1 Phoenix Model 5500-624 Interface Module

2.2.2 Equipment Setup

Follow the setup procedures given in section 2.1.2 for the FRAMED T1 FORMAT screen with the following exceptions:

IMPEDANCE: Using the SoftKey select **BRDG.** This allows the 5500 to be connected across the terminated T1 line.



The FRAMED T1 FORMAT screen will appear as above after changing from TERM to BRDG. Press the menu down key one time to select the FRAMED T1 BERT screen. On this menu changes will be made to view parameters that are meaningful to bipolar violation error monitoring.

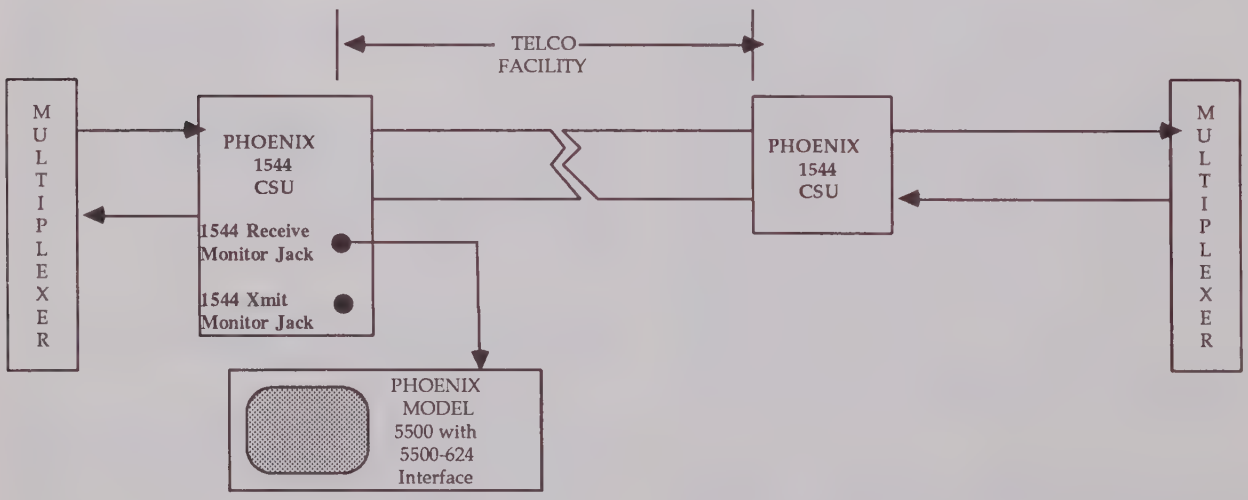
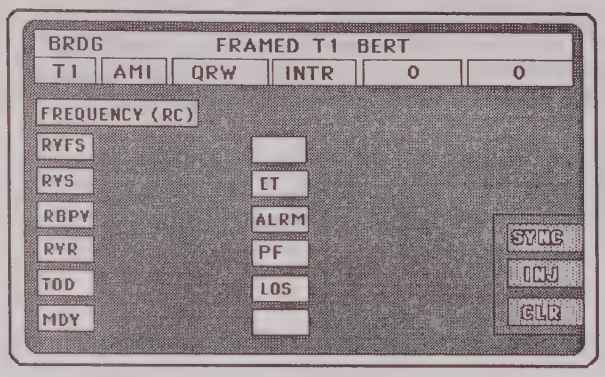


Figure 2-2. T1 Bipolar Violation Monitoring with Phoenix 5500



Observing the top line of the screen it is seen that the change from terminate to bridge that was made on the previous screen is reflected on this screen in the upper left cornor.

Use the **CURSOR** key to move the cusor over the top left field. Use the **SELECT** key to scroll the parameter field until RVFS appears in this field. This field will provide a count of the number of seconds in which no violations occured on the receive pair of the T1 line under test.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECET** key to scroll the parameter field until RVS appears in the field. This field will provide a count of each second in which at least one receive violation occurs.

Use the **CURSOR** key to move down three fields (RBPV and RVR should still be set from the previous setup). Use the **SELECT** key to scroll the parameter field until TOD appears in the field. This parameter is a time-of-day clock which shows the time in hours, minutes, and seconds. It is most useful when operating the 5500 with a printer as the exact time is then printed on the test results for future reference.

Use the **CURSOR** key to move the cursor down one field. Use the **SELECT** key to scroll the parameter field until MDY appears in the field. This field will present the month, day, and year. This parameter is generally used with TOD to imprint the printer output for indentification.

Use the **CURSOR** key to move the cursor one field to the right. Use the **SELECT** key to scroll the parameter field to [ ] (blank). Use the **CURSOR** key to move the cursor to the top right parameter field. Use the **SELECT** key to scroll the parameter field to [ ] (blank). The screen should now appear as shown above and the 5500 is ready to begin bipolar violation monitoring.

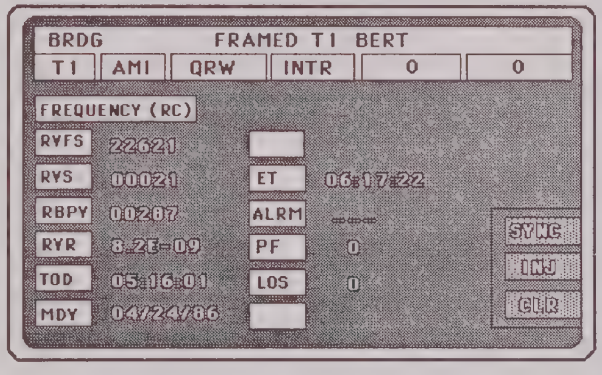
2.2.3 Test Performance

Ensure that the Model 5500 is connected to the near end CSU as shown in figure 2-2. Press the **CLR** softkey to set all the internal counters in the 5500 to zero. Press the **RUN/STOP** switch on the front panel of the 5500. The 5500 should gain synchronization and begin tracking bipolar violations. This is indicated by the illumination of the SYNC led on the front panel.

If the SYNC led does not illuminate, recheck all connections and switch settings. (Refer to table 3-2 on (T1) Page 9 in the options section of this instruction book.)

2.2.4 Test Result Evaluation

After the test period has been completed, or for that matter, at any time during the test, the operator may observe the 5500 CRT display to evaluate the performance of the T1 link under analysis. At this time the display might appear as follows:



From the above display the following information can be obtained.

The test has been completed (RUN is no longer displayed in upper right corner of the display) and the 5500 is no longer in sync (SYNC light on front panel is off and SYNC appears half intensity on display).

The test ran for 6 hours, 17 minutes and 22 seconds (ET parameter).

The current date is April 24, 1986 (MDY parameter) and the current time is 5:16:01 AM (TOD parameter).

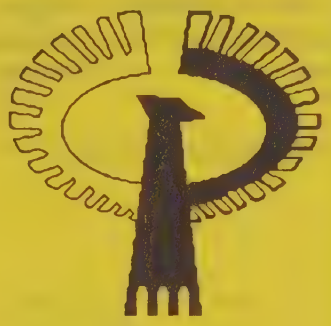
Neither sync nor power was lost during the test (LOS and PF parameters).

During the time of the test there were 22,621 seconds in which there were no errors (RVFS parameter). There were 21 seconds in which at least one error occured (RVS parameter).

There were a total of 287 bipolar violations on the receive line during the test (RBPV parameter) which worked out to a 8.2E-9 receive violation rate (RVR parameter).

User Notes

5500
Data Communications
Analyzer



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5.1 GENERAL

The Model 5500 Data Communications Analyzer is a high speed test set composed of a chassis, power supply, and four printed circuit boards. The four PC boards are the 5500 control board, video control board, front panel display/keypad board, and an interface board. The interface board may be one of several plug-in modules, allowing the 5500 to operate in a variety of configurations. Figure 5-1 is a block diagram of the 5500 and illustrates the inter-connection between the boards.

In addition, two optional boards are available, one to perform jitter measurements on received data, and the other to provide highly stable clocks (1PPM) sources.

Each 5500 is supplied with a 9V NI-CAD battery and necessary control logic to back up the read/write memory during power down.

5.2 5500 CONTROL BOARD

The 5500 control board is the largest PW Board in the system, and contains most of the systems intelligence. This board contains the control processor, 96K bytes of ROM, and 24K bytes of battery backed RAM. There are five separate crystal controlled oscillators on this board for timing the various functions of the 5500 systems. Most of these oscillators, along with software controlled counters and selectors, are used for generating bit rate clocks necessary for data signal element timing.

LSI counter/timer integrated circuits are used extensively on this board for software controlled functions such as frequency and event timing measurements.

Time of day and calendar functions are maintained by an integrated circuit which is battery backed during system power down.

The functions associated with bit error testing are performed by a combination of programmable array logic and MSI. Seven different psuedo random pattern sequences may be generated and clocked out to the installed interface board, at the selected clock rate. The clock rate may be from 75 bps to 13 Mbps.

In addition to the pseudo random pattern, several fixed patterns, or a user controlled pattern may be loaded into a memory buffer, and clocked out the installed interface at the selected clock rate.

The 5500 control board has the logic to interface the video control board, the selected interface board, and the optional low speed jitter.

There are two remote control ports. One of these is RS-232 compatible while the other is IEEE-488. These ports allow complete control of the 5500 by a wide range of controllers including computers, video terminal modems, etc. Additionally, the RS-232 port may be configured to drive a printer for unattended test data recording.

5.2.1 Component Functions

Table 5-1 relates IC's and other parts to functions of the 5500 control board. This could be helpful in localizing a problem.

5.2.2 Troubleshooting

If a 5500 control board is suspected to be malfunctioning, a few basic checks can be made to isolate the malfunction. The following steps should be followed:

1. DC Voltage Measurement

POTENTIAL	J8-Pin(s)	Tolerence (+/-)
+5 V	3,4,5	.25V
+12 V	10	.6V
-12 V	11	.6V
-5 V	1,2	.25V
-30 V	12	5.0V
Ground	6,7,8,9	

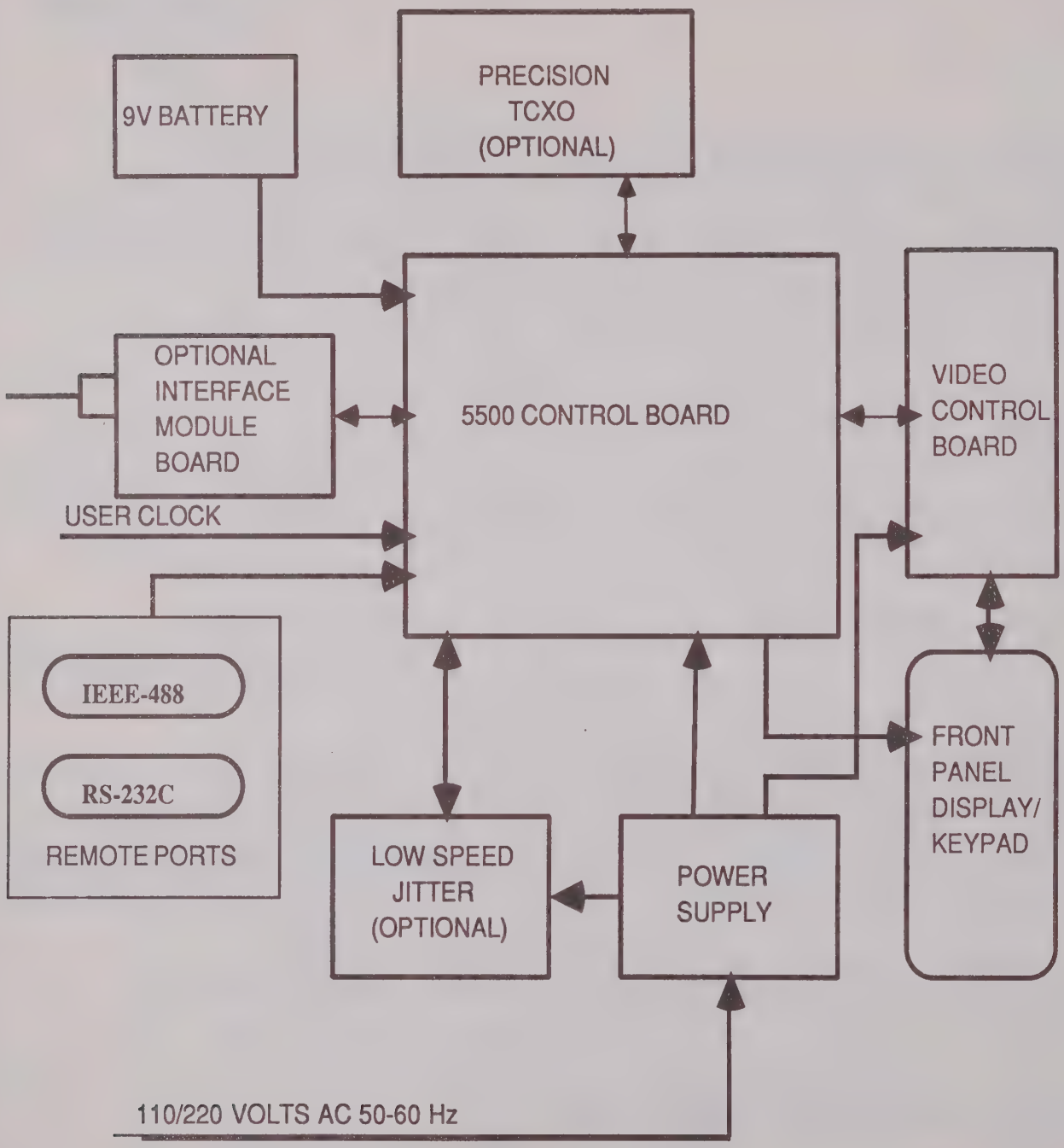


Figure 5-1. 5500 Block Diagram

Table 5-1. 5500 Control Board Components

IC/IC's	FUNCTION
U54	Control Processor
U55, U56, U57	PROM
U58, U59, U60	RAM
U74, U93	CHIP Select Decoder
U89, U90, U91	IEEE 488 Bus Control and Interface
U88, U96, U97	RS232 Remote Port Control and Interface
U86, U87, U85, U95	Bit Rate Selector
U83, U67, U63, U64	Frequency Measurement
U62, U52, U68	Event Timing Measurement
U30, Y5	Time of Day Clock & Crystal
U44, U45, U47, U46	User and Fixed Pattern Buffer and Output Control
U23, U26, U24, U4, U3, U66	User and Fixed Pattern Compare Buffer and Input Control
U7, U8, U9, U15	Pseudo Random Pattern Generator (Pattern to be Transmitted)
U36, U37	Transmit USART
U65, U77, U78	Bit Error Injection Logic
U27, U28	Bit Error Test Control Interface
U10, U11, U12, U34	Pseudo Random Pattern Generator (Pattern Compared to Received Data)
U40, U43	Receive USART
U31, U32, U33	Receive Shift Register
U16, U17, U18, U19	Receive Data Comparator
U53, U69, U35, U14	Bit Counters & Bit Error Counters
U13	Pattern Sync Acquisition Logic
U20	Pattern Sync Loss Logic
J4	Connects to Optional Low Speed Jitter Board
J8	Power Supply
P3	9V Battery Connector
J2	IEEE 488 Port
J1	RS232 Remote Port
P4	User Clock Port

Table 5-1. 5500 Board Components (Cont)

IC/IC's	FUNCTION
J5	To Interface Option Board
P6	To Front Panel Board
J6	To Video Control Board
Q7, Q8, Q9, Y1	6.176 Mhz Crystal Controlled Oscillator
Q10, Q11, Q12, Y2	6.144 Mhz Crystal Controlled Oscillator
Q16, Q17, Q18, Y4	Optional Crystal Controlled Oscillator
Q13, Q14, Q15, Y3	4.068 MHz Crystal Controlled Oscillator
Y5	4.194304 MHz Crystal for Calendar Clock

2. Oscillator Frequency Measurements

The following oscillators may be checked with a suitable frequency counter such as a HP5315A or HP5316A, with a high impedance probe. All frequencies should be within 50 ppm of desired frequency.

4.068 Mhz between Gnd TP and Collector of Q13.

6.176 Mhz between Gnd TP and Collector of Q7.

6.144 Mhz between Gnd TP and Collector of Q10.

Optional Osc between Gnd TP and Collector of Q16.

3. Visual Check

A visual check of the board could reveal possible broken parts or components dislodged from sockets due to rough shipping and handling.

4. Board Replacement

Further troubleshooting, beyond the three basic checks previously described, is not recommended. Replacement of the PC board can be accomplished by carefully removing all connectors and six mounting screws and removing the board from the chassis. Reverse the removal procedure to install a known good spare. Extreme care should be exercised when removing and replacing connectors, so as not to bend pins or offset the connector. The defective board may be returned to Phoenix Microsystems for repair.

5.3 5500 VIDEO CONTROLLER BOARD

The video control board buffers the display data transferred from the 5500 control board, and translates the text data to a series of video dots to be displayed on the CRT. This board also provides raster synchronization for the CRT.

A secondary function performed by the video controller is scanning the front panel keyboard and translating depressed keys into a suitable code for the 5500 control board.

The video board has its own control processor and ROM. A RAM is shared by the control processor and a special video processor chip. The control processor writes display data into the RAM under command from the 5500 control board. The special video processor retrieves the data from the RAM on a time shared basis, to produce the video data for the CRT. Other components on the board are used for timing, temporary buffering, and character code translations.

5.3.1 Component Functions

Table 5-2 relates specific parts on the board to the particular function it performs.

5.3.2 Troubleshooting

As with the 5500 control board, it is recommended that

Table 5-2. Video Controller Board Components

COMPONENT	FUNCTION
U3	Video Control Processor
U4	Program ROM
U5	Buffer RAM
U15	Video Processors
U14, U24	Row Buffers
U26	Character Generator
U23	Video Attribute Controller
Q1, Q2, Q3,	Video Dot Clock Oscillator
U1, U6, U7,	5500 Control Board Interface Connectors
P1	5500 Control Board Interface
P2	Display/Keyboard Interface
P5	CRT Interface Connector
P4	Composite Video Connector
P6	Brightness Control Pot Connector
P3	Power Supply Connector
R25	Half Intensity Level Adjustment for composite video signal. (Alt Video)
R22	Half Intensity Level Adjustment for 5500 CRT.

troubleshooting of this board be limited to visual inspections, voltage checks and oscillator frequency measurements. Problems beyond this should be solved by board replacement, and returning the defective unit to Phoenix Microsystems for repair.

1. DC Voltage Checks

POTENTIAL	P3 Pin(s)	TOLERENCE
+5 V	1,2	.25V
+12 V	7	.25V
GROUND (GND)	3,4,5	

2. Oscillator Check

   8.064 Mhz + 50 ppm between Q1 collector and Gnd

5.3.3 Adjustments

The CRT brightness may be adjusted using the potentiometer on the 5500 back panel.

Half intensity can be adjusted for the 5500 CRT by rotating potentiometer R22 on the video control board. Half intensity for an optional video monitor may be adjusted with R25 on video control board.

5.6.4 Fuse Replacement

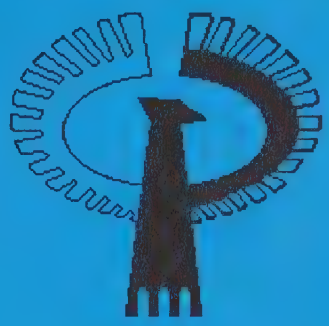
The three dc fuses are mounted on the power supply printed circuit board near the edge of the board. The fuse nearest the board edge is the +5V, with +12V next in order and -12, -5 being the one nearest the center of the board. Replace fuses only with ones of equal current ratings.

5.6.5 Troubleshooting

Due to the compact nature of the power supply module, it is not recommended that field repair be performed. With a spare module replacement, it should be a simple matter to determine if a unit is defective. The defective unit should be returned to Phoenix Microsystems for repair.

User Notes:

5500
Data Communications Analyzer



Phoenix microsystems

Phoenix Instruction Book

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options

THIS SECTION CONTAINS INSTRUCTIONS ON THE FOLLOWING OPTIONS:

Model 5500-200 RS-232C Interface Module
Model 5500-300 CCITT V.35 Interface Module
Model 5500-400 RS-449 Interface Module
Model 5500-450 RS-449/MIL-188C-114 Interface Module
Model 5500-500 TTL Interface Module
Model 5500-555 MSU I/O Control Module
Model 5500-MSU Module Switching Unit
Model 5500-600 DS1/DS1C Interface Module
Model 5500-624 DS1 (T1) Interface Module
Model 5500-700 T-2 Interface Module
Model 5500-800 CCITT G.703 2.048 Mbps Interface Module
Model 5500-805 CCITT G.703 8.448 Mbps Interface Module
Model 5500-J01 Low Speed Jitter Option
Model 5500-J02 High Speed Jitter (T1) Option
Model 5501 G821 Performance Evaluation

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Model 5500-200

RS-232C Interface Module

1.0 INTRODUCTION

This section details the operation of the Model 5500-200 RS-232 Interface Module option. The logic required to operate in SYNC and ASYNC mode is located within the Model 5500 itself, therefore the interface module performs only the mechanical and electrical interfacing of the EIA RS-232 standard signals to the TTL level signals used within the Model 5500. DCE or DTE emulation, and SYNC or ASYNC mode operation are controlled and switchable from the Model 5500 front panel keys, or by commands over the remote ports.

2.0 DESCRIPTION

Table 2-1 presents the Model 5500-200 RS-232 Interface Module specifications.

Table 2-1. Model 5500-200 Specifications

CHARACTERISTIC	SPECIFICATION
Modes	Synchronous or Asynchronous
Emulation	DCE or DTE
Data Rates	50 bps to 20.0 kbps per EIA RS-232C
Character Size	5, 6, 7, 8 data bits
Parity	Odd, Even, or no parity bit
Stop Bits	1 or 2 bits
Input Data Characteristics	Mark signal, binary state 1, or OFF = -3 Volts Min.
	SPACE signal, binary state 0, or ON = +3 Volts Min.
Line Drivers	Output Voltage: Selection of ±5.5 ±.5V peak for worst case MODEM testing or ±9.0 ±2.0V peak for normal BER testing. Selection is made by strap options on the RS-232 interface module.
	Factory set for nominal ±9.0 V. ±2.0 V. operation.
	Output Impedance: 300 ohms minimum
	Slew Rate: 30.0 volts per microsecond maximum.
	Short-circuit Current: 12 milliamps maximum.

Table 2-1. Model 5500-200 Specifications (Cont)

CHARACTERISTIC	SPECIFICATION
Line Receiver	Maximum Input Voltage: ± 25 Volts Load Impedance: 3000 ohms min. to 7000 ohms max. MARK Voltage: 0.0 Volts Max. SPACE Voltage: 2.0 Volts Min.

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-200 RS-232C interface is capable of operation in Synchronous and Asynchronous modes with both DCE and DTE configuration. The module has two 25 pin subminiature 'D' type connectors; normally Male for DCE and Female for DTE. In addition, the DCE/DTE emulation is electronically switchable from the Model 5500 front panel or via command over either remote control port. Figure 2-1 presents a simplified block diagram of the Model 5500-200 module. Table 2-2 presents the RS-232 connector pin assignments.

3.0 OPERATION

3.1 DATA TERMINAL EQUIPMENT (DTE) CONFIGURATION

The Model 5500 may be configured as Data Terminal Equipment (DTE) for testing Data Communications Equipment (DCE) such as Modems, Multiplexers, or other peripheral equipments configured as DCE. This is accomplished by toggling the front panel key labeled 'DCE/DTE' until DTE appears in the upper left hand corner of the BERT CRT display (refer to section 3.2 of this instruction book for location and description of the Model 5500 controls and indicators). In the synchronous mode of operation the Model 5500 maybe set to derive clock from the equipment under test or it may generate the clock internally and provide it to the equipment under test.

In the asynchronous mode of operation, data is transmitted and received without a clock. Start and stop bits provide proper decoding of the data bits in each character (byte) sent while timing is extracted from the bit transition. In Synchronous operation, with the DCE under test acting as the source of timing, the Model 5500 bit rate selection should be set to EXTERNAL. In this position the Model 5500 will derive clock from pin 15 (Transmission signal Element timing-DCE Source) of the DTE I/O connector on the interface module. Transmit data and clock are available on pins 2 and 24 respectively, and receive data and clock are available on pins 3 and 17 respectively.

If a Bit Rate is selected on the Model 5500 then the internal generator of the test set supplies the clock signal to the equipment under test. If the user desires to test at a non-standard bit rate the unit can also be operated with an externally applied USER CLOCK into the rear panel BNC connector with the Model 5500 Bit Rate field set to USER. The frequency of this externally applied clock is read on the CRT display by scrolling through the frequency selections to the appropriate option-either TC or BR.

In either case the test set ignores signals present on pin 15 of the I/O connector. Transmit data and clock are on pins 2 and 24. Receive data and clock are on pins 3 and 17, respectively.

When operated in an Asynchronous mode the Model 5500 bit rates are internally generated. The appropriate character size, number of stop bits, and parity must also be selected using the front panel cursor and select keys. In this mode of operation no clock signals are transmitted. Transmit data appears on pin 2 and Receive data on pin 3 of the I/O connector. Any signals appearing on pins 15 and 17 are ignored. The Model 5500 recovers clock from the received data transitions to provide internal synchronization to the received patterns.

3.1.1 Controls and Indicators

Model 5500 front panel keys labeled RTS/DCD and DTR/DSR enable the user to turn RTS and DTR ON and OFF when the Model 5500 is configured as a DTE.

Table 2-2. RS-232 Connector Pin Assignments

Pin Number	Interchange Circuit	C.C.I.T.T. Equivalent	Description	Gnd	Data		Control		Timing	
					From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	AA	101	Protective Ground	X						
2	BA	103	Transmitted Data			X				
3	BB	104	Received Data		X					
4	CA	105	Request to Send					X		
5	CB	106	Clear to Send				X			
6	CC	107	Data Set Ready				X			
7	AB	102	Signal Ground (Common Return)	X						
8	CF	109	Received Line Signal Detector				X			
9			(Reserved for Data Set Testing)							
10			(Reserved for Data Set Testing)							
11			Unassigned							
12	SCF	122	Sec. Rec'd. Line Signal Detector				X			
13	SCB	121	Sec. Clear to Send				X			
14	SBA	118	Secondary Transmitted Data			X				
15	DB	114	Sig. Element Timing (DCE Source)						X	
16	SBB	119	Secondary Received Data		X					
17	DD	115	Rec. Sig. Element Timing (DCE Source)						X	
18			Unassigned							
19	SCA	120	Secondary Request to Send					X		
20	CD	108.2	Data Terminal Ready					X		
21	CG	110	Signal Quality Detector				X			
22	CE	125	Ring Indicator				X			
23	CH/CI	111/112	Data Signal Rate Selector (DTE/DCE Source)				X	X		
24	DA	113	Xmit. Sig. Element Timing (DTE Source)							X
25			Unassigned							

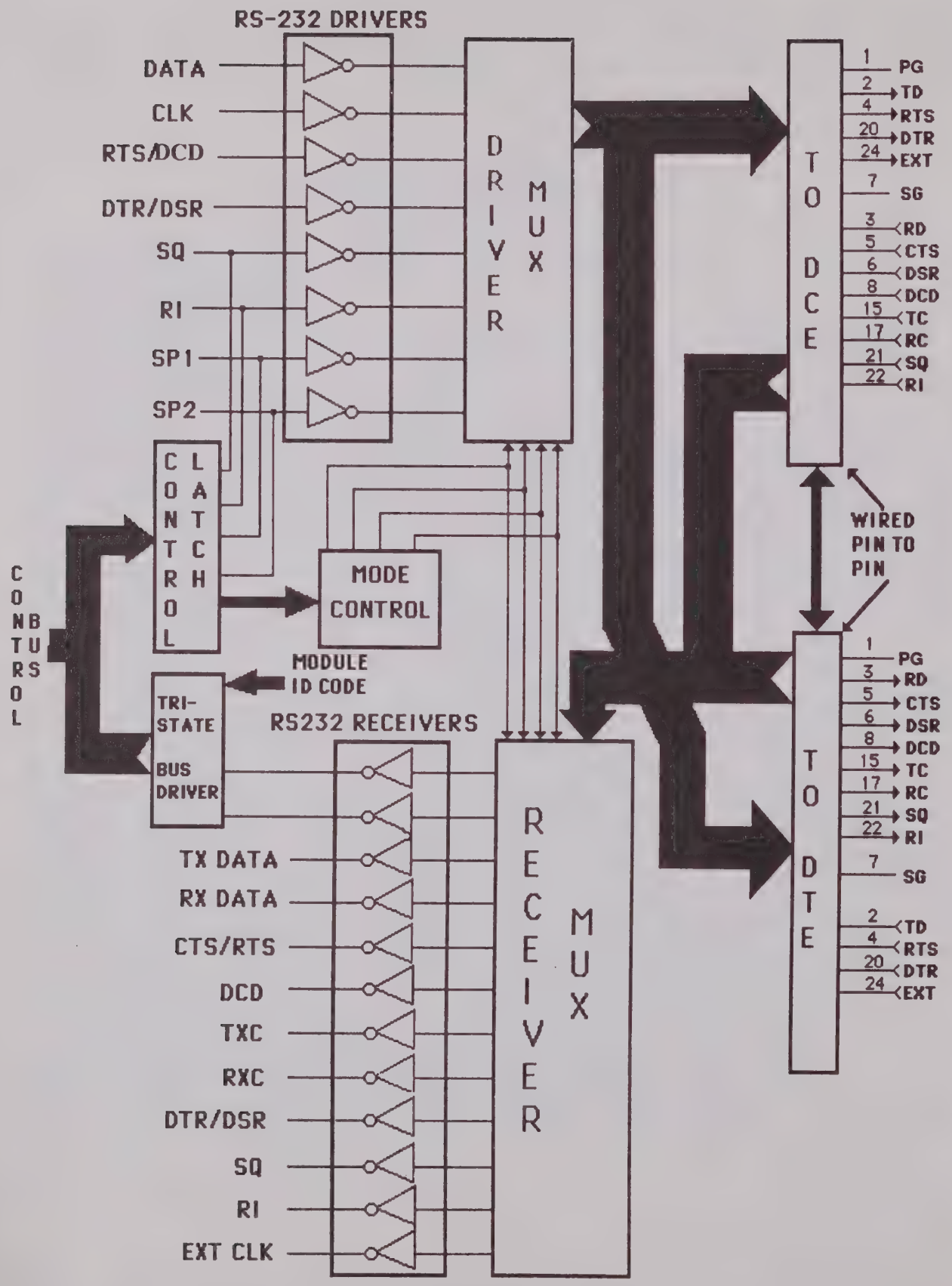

Figure 2-1. Model 5500-200 RS-232C Interface Module Block Diagram

Twelve green LED's provide visual indication of the primary lead status as follows:

Transmit Data - (TD)
Receive Data - (RD)
Transmit Clock - (TC)
Receive Clock - (RC)
Request to Send - (RTS)
Clear to Send - (CTS)
Data Set Ready - (DSR)
Data Terminal Ready - (DTR)
Data Carrier Detect - (DCD)
Ring Indication - (RI)
Signal Quality - (SQ)
Transmit Clock External - (SCTE).

The front panel key labeled DCE/DTE electronically switches the rear panel I/O Connector functions from DCE to DTE and vice versa. This eliminates the need for special cables to use with the RS-232 interface module. These and any other functions, and indications may accomplished and displayed at a remote terminal using the RS-232 or IEEE-488 remote control ports.

3.2 DATA COMMUNICATIONS EQUIPMENT (DCE) CONFIGURATION

The Model 5500 may also be configured to operate as a DCE by toggling the DCE/DTE front panel key until the DCE indication appears in the upper left hand corner of the CRT display. Again, either synchronous or asynchronous peripherals can be tested as in the DTE configuration.

In synchronous mode, the Model 5500 may derive clock from the DTE under test or supply clock to the equipment from its own internal generator. When set to EXTERNAL CLOCK, the Model 5500 receives timing from the DTE Transmit Signal Element Timing on pin 24 of the rear panel DTE I/O connector. The frequency of the external clock is read on the CRT display by scrolling through the frequency selections to XC. Under this condition the Transmit Data on pin 2 and Transmit Signal Element timing on pin 24 are analyzed by the model 5500.

The Model 5500 generates Receive Data on pin 3 and Receive Signal Element timing on pin 17 in accordance with the DTE supplied clock on pin 24.

If it is desired to have the Model 5500 supply clock for the equipment under test it is necessary to select the desired bit rate instead of EXTERNAL. In this case, the model 5500 supplies timing to the DTE under test on pin 15 of the I/O connector. The Model 5500 analyzes the Transmit Data on pin 2 and Transmit signal timing on pin15. Receive Data on pin 3 and Receive Signal Element timing on pin 17 are generated from the Model 5500 internal clock source. A user supplied external clock signal into the USER CLOCK BNC jack will cause the Model 5500 to generate data and clock at the externally applied clock rate when the Model 5500 is set to USER in the BIT RATE field.

Asynchronous DCE mode operation of the Model 5500 requires selection of the ASYNC mode, bit rate, character size, parity, and number of stop bits. Data is generated and received in character format with no clock signals provided.

Timing is derived from the data transitions and the start and stop bits location identifies the data (character) and parity bits to the receiver for proper decoding.

3.2.1 Controls and Indicators

Front panels keys are available which enable the user to turn Data Set Ready (DSR) and Data Carrier Detect (DCD) "ON" and "OFF" in the DCE mode operation. In addition, these conditions, and any other settings can also be controlled from a remote terminal using the RS-232 or IEEE-488 rear panel remote control ports.

The twelve green LED indicators provide status of the primary interface signal leads as discussed earlier in section 3.1.1.

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Model 5500-624

DS1 (T1) Interface Module

1.0 INTRODUCTION

The Model 5500-624 DS1 (T1) Interface Module enables the Model 5500 to test all types of T-1 Carrier equipments with D4 Superframe Format Framed patterns or Unframed patterns. This feature permits the user to test digital switches, digital access and cross-connect systems, and other devices requiring a framed pattern for test purposes, as well as repeatered lines, multiplexers, channel banks, and Channel Service Units with unframed pattern requirements. The line format is selectable for either AMI or B8ZS. The module functions for signals at normal transmit and receive levels, as well as monitor level signals at the DSX points.

The Model 5500-624 also accepts the Model 5500-J02 Jitter Measurement and Injection Option. The J02 option hardware consists of a PC board which plugs into a special connector on the Model 5500-624 PC board.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-624 DS1 (T1) Interface Module.

Table 2-1. Model 5500-624 Specifications

CHARACTERISTIC	SPECIFICATION
Pulse Rate	1.544 Mbps ±50 ppm Max.
Output Pulse Amplitude	±3.0 V ±10% Into 100 ohms
Output Pulse Width	324 ±30 nsec at 50 percent amplitude
Rise and Fall Times	50 nsec ±25 nsec (10-90%)
Overshoot	Less than 10% of amplitude height.
Reveiver Input	0.5V TO 6.0V peak, ALBO (Automatic Line Build Out) allows operation with up to 4000 feet of PIC22 cable between unit and source.
Input Impedance	100 ohms ±5% terminated. Greater than 1K ohms bridged.

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-624 Framed/Unframed Interface Module enables the Model 5500 to generate and receive T1 serial data streams, recover clock, and regenerate data from low level signals. The mechanical interface between the module and the system under test consists of miniature (bantam) jacks for Transmit, Receive, and a 15 pin subminiature D type connector wired in parallel with the TX and RX bantam jacks.

The Generator section (see figure 2-1) consists of a TX clock select MUX, TX framing logic, a line encoder for AMI or B8ZS, and a bipolar line driver. The Receiver has a switchable line termination of 100 ohms which is disconnected for the high impedance BRDG (Bridge) mode. The receiver section includes an ALBO (Automatic Line Build Out circuit), and Clock Recovery/Data Detector which provide recovered clock and data to the line decoder and RX Frame Sync Logic.

The Line Decoder is set to AMI or B8ZS as appropriate and converts the line coded signal to a TTL level bit stream for analysis by the Model 5500 internal logic. The BPV detector compares the output of the Data Detector to the AMI coding rule and passes information on violations of the rule to both the line Decoder and Counter Timer circuits which in turn initiate the count of BPV's displayed on the CRT.

In the B8ZS mode of operation the Line Decoder and Bipolar Violation Detector recognize the intentional Bipolar Violations found in B8ZS substitutions for strings of eight zeros.

All BPV's that are not associated with a valid B8ZS substitution are counted and displayed as BPV errors.

2.1.1 D4 Framing

The transmit and receive data may be either Framed or Unframed, as selected on the FORMAT Menu. In the Framed mode, the four test points accessible at the rear connector panel of the interface module provide "RX S BIT", "RX S BIT CLK", "TX S STB", and "TX MF SYNC" D4 Framing sync signals. The RX Frame Sync Logic provides D4 Framing Status information regardless of the Terminate/Bridge mode of the 5500. This feature is particularly useful in monitoring live traffic because it provides indication of the Framed/Unframed status of the monitored line and also identifies "F" Bit error, "S" Bit errors, loss of carrier (no bipolar pulses on the line) and "B2" ALARM (all Bit 2's = 0). This Framing Status data is combined and displayed as the "ALARM" parameter on the BERT menu.

Table 2-2 presents a summary of the "ALARM" display conditions:

Table 2-2. Alarm Display Conditions

DISPLAY	CONDITION
DISPLAY	**CONDITION**
ALRM.....	D4 Framed with no Framing Anomalies
ALRM.....F	The letter "F" in right hand position indicates the signal is not D4 framed. If the "F" is intermittently displayed, it indicates Framing errors on a D4 signal.
ALRM .....C..	Loss of Carrier (No RX Signal)
ALRM ...S....	"S" Bit Errors (alternate 193rd D4 bits are called "S" Bits).
ALRM B2.....	"B2" or "Yellow Alarm", all Bit 2's (in each DS0 channel byte) are zero.
	NOTE: These status/alarm conditions may occur in combination; their positions will always be the same. For example, alarms indicating "yellow alarm", "S" bit errors, loss of carrier , and frame errors would yield a display of: ALRM B2.S.C.F

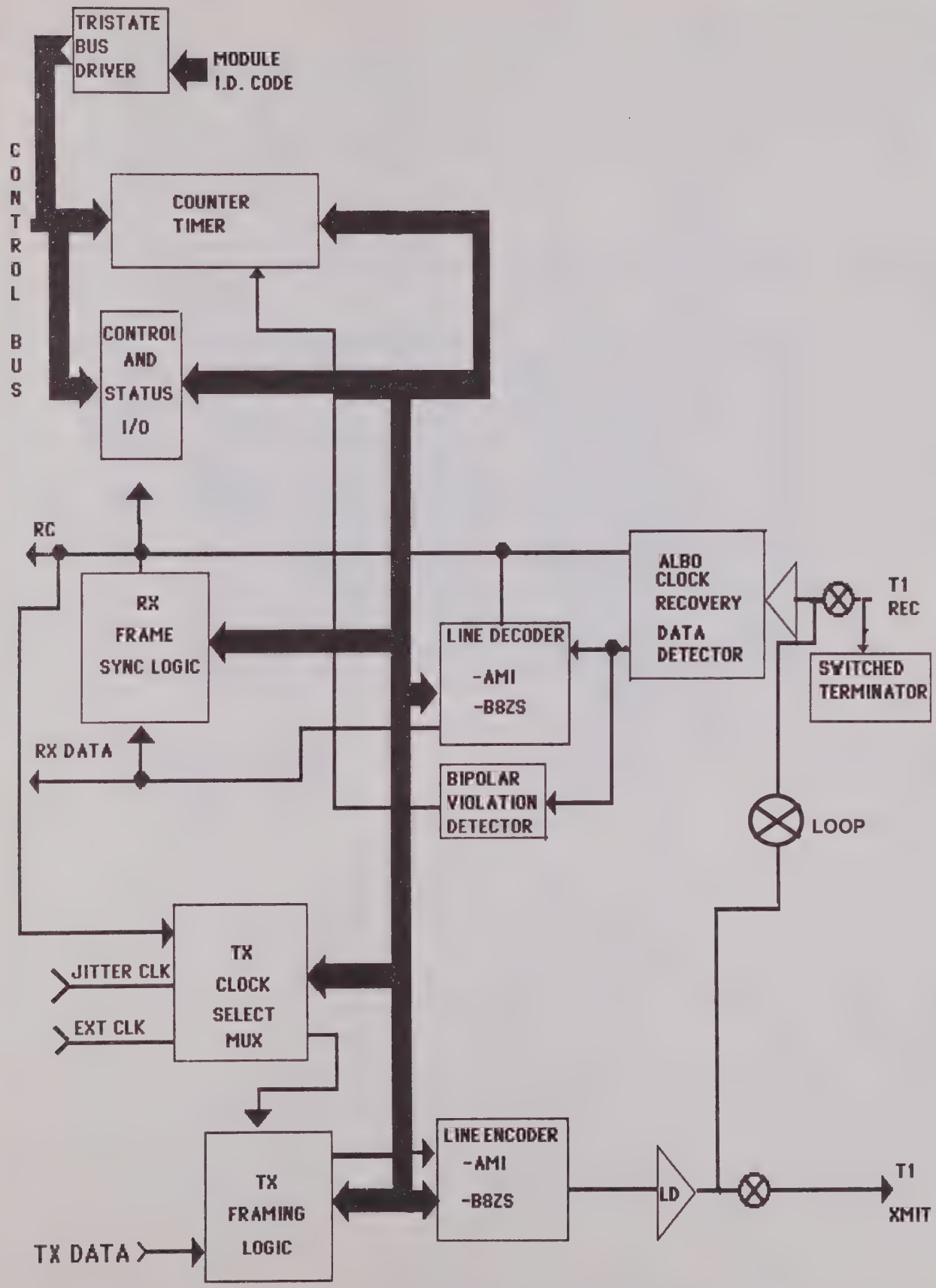


Figure 2-1. Model 5500-624 Interface Module Block Diagram

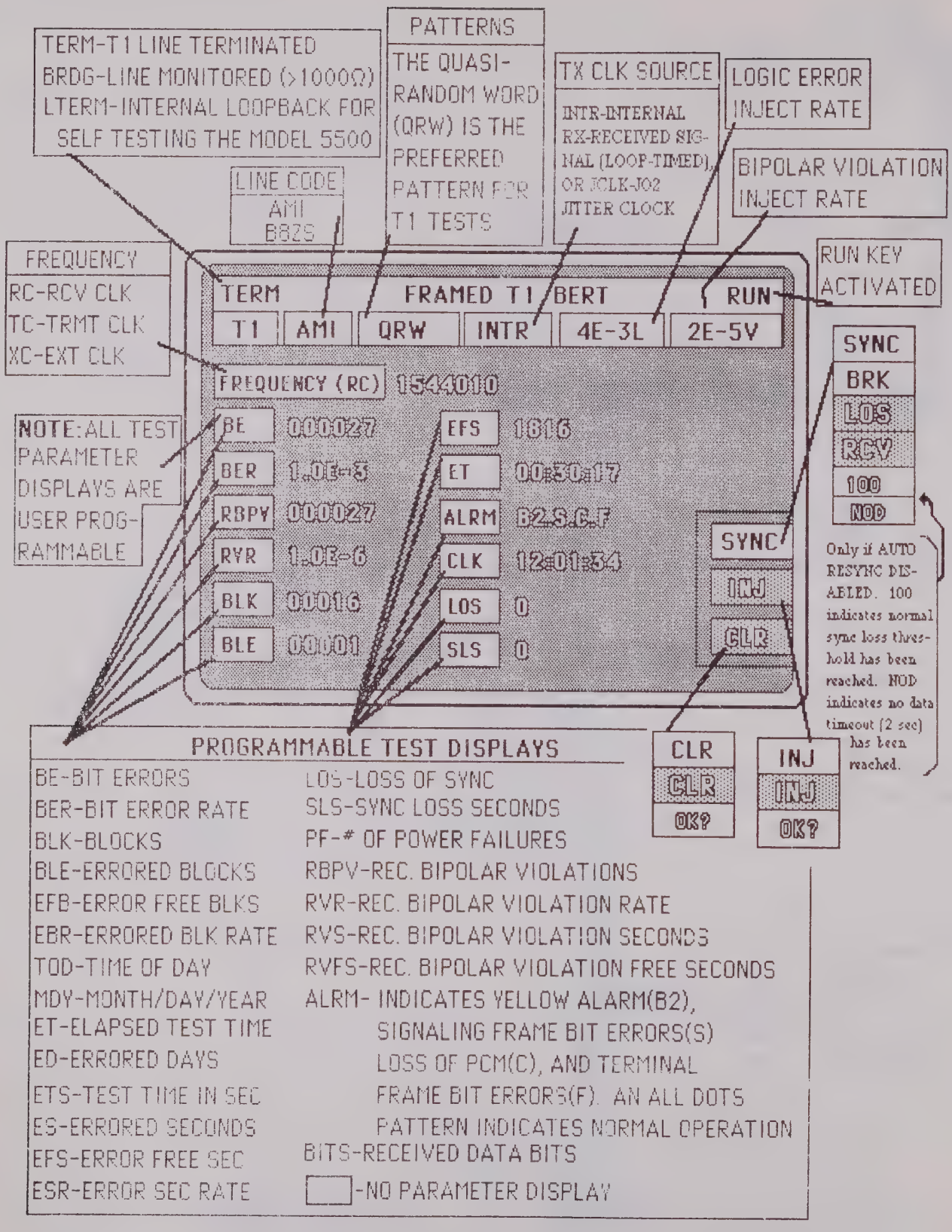


Figure 3-1. T1 Framed BERT Display

3.0 OPERATION

3.1 LOGIC/BPV ERROR INJECT/MEASURE

The 5500-624 Interface Module allows independent injection of BPV's and logic errors in the transmitted data. BPV inject rates are selectable from 2^{-3} to 1^{-7} and O (disable); logic error inject rates are selectable from 9^{-3} to 1^{-9} and O (disable). Rate control is independent, allowing injection of both BPV's and logic errors, only BPV's, only logic errors, or neither. Likewise, BPV's and logic errors are measured and displayed separately. While received logic errors are valid only when the selected pseudo random pattern is being received, the BPV parameter is valid for all received bipolar signals, including "live" traffic, as long as the proper line code (AMI or B8ZS) is selected.

3.2 TRANSMIT CLOCK SOURCE

The 5500-624 module allows three different clock sources to be used for transmit timing:

- o Internal Clock (5500 1.544 Mhz Crystal Clock)
- o Rx (Clock recovered from Rx received data input)
- o Jitter (Jitter clock source from the JO2 Jittter Option Board).

Normal operation requires use of the Internal Clock. The Rx clock can only be used when the Receive Data Timing source is independently or "network" timed (Selection of Rx clock source when the 5500 transmit data is looped back to the 5500 receiver will not operate properly; in that mode the clock recovery circuit would in effect be chasing itself and would be very unstable and out of tolerance).

The Jitter clock source is used only when the JO2 Jitter option board is injecting jitter into the transmitted data output.

Clock source selection is via the FORMAT menu.

3.3 BERT FORMAT DEFINITIONS

Table 3-1 presents the T-Carrier BERT Format definitions that are unique to the Model 5500-624 Interface Module.

3.4 BER TEST ASSISTANCE

Table 3-2 presents a list of possible proablem areas if the Model 5500 does not achieve synchronization with the device under test.

Table 3-1. BERT Format Definitions

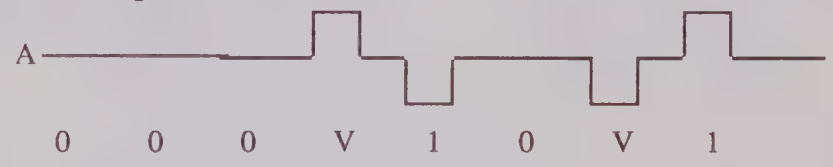
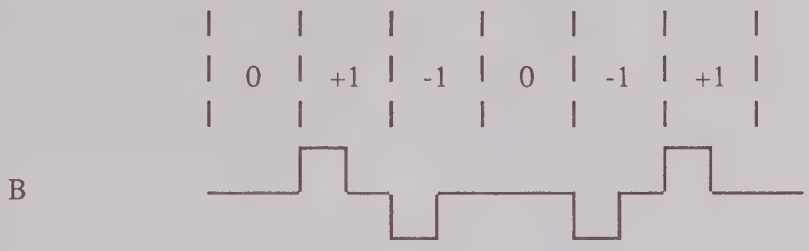
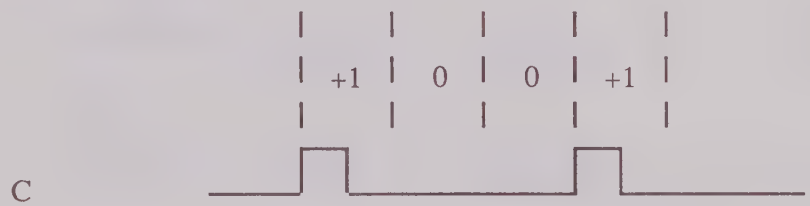
ITEM	DEFINITION
LINE RATE	This block displays the line rate as T1, T1C, or T2 for U.S. systems or 2.048 and 8.448 Mbps for CCITT G.703 modules. This is not a selectable parameter but is fixed by the interface module inserted into the Model 5500. It is a convenience item to remind the operator of the rate at which the Model 5500 is testing.
LINE CODE	The line code of the T-Carrier system under test may be selected by moving the half intensity block over the LINE CODE window and using the SELECT keys to choose the options. The options are: T1 AMI or B8ZS T1C AMI or B8ZS T2 AMI or B6ZS 2.048 Mbps AMI or HDB3 * * 2.048 Mbps G.703 modules are set for HDB3 at the factory. A DIP switch on the module allows selection of AMI coding. The Alternate Mark Inversion (AMI) or Bipolar line code is the line code currently in use in the U.S. on all T1 baseband source code into AMI line code. Note that successive MARKS (1's) always alternate in polarity. A new format, Bipolar 8 Zero Substitution (B8ZS), is being considered for T1 in order to remove the restrictions on the number of successive SPACES (0's) which AMI places on the source coder. While not in actual use at the present time, this line code may become the future standard. An example of a B8ZS coded signal is provided in figure A.  Assuming the last 1 transmitted was a positive "one". The polarities of the substituted word are simply reversed if the last "one was negative. 0 0 0 0 0 0 0 0 original word 0 0 0 +1 -1 0 -1 +1 substituted word BPV's always occur at the 4th and 7th bit positions of the substituted word. The line code used by T2 carrier systems is B6ZS which is similar to the B8ZS code previously discussed but which limits strings of 0's to less than 6. In this case a block of six consecutive zeros is substituted by the sequence "0 + - 0 - +" if the preceding mark was positive, or "0 - + 0 + -" if the preceding mark was negative (+ or - represents a positive or negative mark). An example of B6ZS coding is shown in figure B.

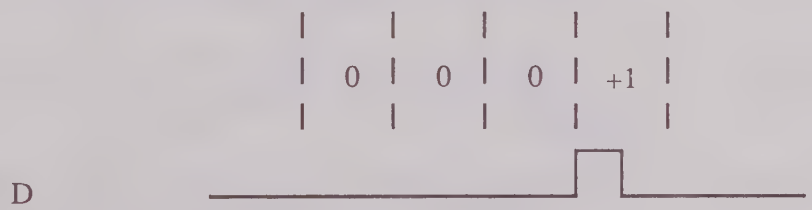
Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION



Finally, High Density, Bipolar 3 Zero Substitution (HDB3) line coding is used in European T-Carrier systems at 2.048 MBPS and 8.448 MBPS line rates. An example of this coding format is shown if figures C and D. (Preceding violation was negative and preceding pulse was negative in figure C and the preceding violation was negative and the preceding pulse was positve in figure D.)





The HDB3 coding process generates positive and negative marks alternately each time a binary logical 1 condition occurs within the message signal. However, unlike AMI coding, the maximum number of consecutive zeros is limited to a value of 3. If a series of 4 consecutive zeros does occur, the 4th zero is replaced by a mark referred to as a VIOLATION. The violation mark is always inserted with the same polarity as the preceding mark. This identifies the departure from the AMI scheme and indicates the occurrence of the violation.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
	In theory, if additional safeguards were not taken, it would be possible for several violations to have an identical polarity, and thus introduce a DC component into the signal. To overcome this problem, the coder continuously monitors the polarity of the last violation (may have been many bits earlier in the data stream) and the polarity of the last mark. The coder then forces the first bit of the 4-bit substitution sequence to a one or a zero, whichever is required, to allow the violation in the fourth bit position to be of opposite polarity to the previous violation.
PATTERN	The pattern choices from the regular FORMAT are all present in T-Carrier FORMAT, but the most useful patterns for T-Carrier testing are:
QRW QUASI-RANDOM WORD	A pattern of (2^20)-1 bits long which has built-in suppression of strings of 0's greater than 14. This pattern is the industry standard for T1 and T1C testing. (2^15)-1: A pseudo-random sequence used in European CCITT G.703 BER testing and jitter testing. (2^20)-1: A pseudo-random sequence of the same length as the QRW, but without the 14 zero suppression. Useful at T2 and for CCITT testing.
MARK	An all 1's pattern which may be used to simulate the "idle" pattern sent out by digital channel banks in an alarm condition.
USER	This is a user definable pattern of up to 135 characters (1080 bits) which could be used to send out patterns with more than 14 zeros or any other pattern a user may want to transmit.
T1 SET	This pattern sends out the standard T1 Channel Service Unit (CSU) loopback code (10000) to cause a remote CSU to loopback for test purposes. This code should be transmitted for 5 seconds before the CSU will loopback to prevent false loopbacks.
T1 RESET	This pattern sends out the standard T1 CSU reset code to return a CSU in loopback to normal operation. The code (100) should be sent out for 5 seconds to reset CSU loopback.
BPV INJ RATE	The user may select any rate of injection of Bipolar Violations from 2^{-3} to 1^{-7} violation/bit. The rate is selected by changing the mantissa from 0 to 9 (a 0 disables the inject function) first and then moving the half intensity block to the right and changing the exponent from -3 to -7 as desired. The select keys or the HEX keypad can be used. A common rate is 1^{-3} which is useful in checking automatic protection switches. Pressing the INJ soft key on the main BERT display activates BPV Injection unless there is a "0" in the BPV inject rate mantissa.
LOGIC ERR RATE	Logic errors are what telephone companies call bit errors to distinguish them from BPV's. This rate of bit error injection is selectable from 9x10-3 to 1x10-9 errors/bit. The errors (and bipolar violations) are uniformly spaced throughout the bit stream when the INJ soft key is pressed. Note that the user is free to have either logic errors or BPV's or both injected.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
CLOCK SOURCE	The user may select from three alternatives depending upon what simulation is being attempted. When the Model 5500 is acting as the generator of the T- Carrier it is normal to choose INTERNAL timing so that the Model 5500 is the master clock. This would be the case whenever any loopback testing is performed. The "RX" or Receive Clock choice allows the user to operate a 5500 in what is called a loop timed mode. That is, the Model 5500 derives clock from the received bit stream and uses this to time its transmitter. This is useful if, for example, the user is making an end to end bit error test with Model 5500's at each end. In this case one of the test sets should be on INTERNAL (acting as the master clock) and the other should be set to RX. The final option available is USER which allows the operator to supply a TTL clock to the rear panel BNC connector. The clock supplied must be at the nominal bit rate of the module being used (i.e. 1.544 MHZ for T1 module, 6.312 MHZ for T2, etc..), and should be at least + 30ppm accurate.

Table 3-2. BER Test Assistance

SYMPTOM	POSSIBLE CAUSE
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Verify that BRIDGE mode in T- Carrier testing has not been selected. (BRIDGE mode disables the Model 5500 transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units.
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.
Test suddenly stops and RUN LED goes off	If continuous testing is desired verify that '0' has been placed in the Number of Blocks test window and press RUN. If testing a specific number of blocks verify that the number of blocks selected has been reached when test set stops. This is normal operation.
Model 5500 display errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. NOTE: T1 carrier systems are only specified to provide a 1x10-6 error/bit rate which is about three errors or less every two seconds.

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Model 5500-J02

T-Carrier Timing (Clock) Jitter Injection/Measurement Option

1.0 INTRODUCTION

The Model 5500-J02 Jitter Injection/Measurement Option is a factory installed option which provides the 5500 user with jitter measurement and jitter injection capability. This capability is used with T-1 1.544 Mbps Bipolar transmission facilities and equipment. The 5500-J02 option consists of a piggy back circuit card which is plugged into the top of the 5500-624 Framed/Unframed T-1 Interface Module (described in the Option section of this instruction book). This option may be installed in equipment of the following configurations:

Model 5500 main frame -- Revision 4.00 or above.

Software -- Revision 4.11 or above.

Model 5500-624 I/O module -- Revision 1.20 or above.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-J02 Jitter option.

Table 2-1. Model 5500-J02 Specifications

CHARACTERISTIC	SPECIFICATION	
JITTER MEASUREMENT		
Bandlimiting Filter	2 pole high pass/8 pole low pass (10Hz to 40kHz)	
Wideband Jitter Amplitude ("TOTAL JITTER")		
Amplitude range	0.00 to 12.75 ui (unit intervals)	
Amplitude accuracy	± 5% ± 0.05 ui	
Narrowband Jitter Amplitude ("CURSOR AMP")		
Amplitude range	0. 00 to 12.75 ui	
Amplitude accuracy	± 5% ± 0.025 ui	
Narrowband Jitter Filter ("CURSOR FREQ")		
	10Hz to 15kHz	15kHz to 40kHz
Center frequency	± 50 ppm	± 50 ppm
Bandwidth (3 dB)	± 11%	± 11%

Table 2-1. Model 5500-J02 Specifications (Cont.)

CHARACTERISTIC	SPECIFICATION
JITTER GENERATOR	
Amplitude Range	0.00 to 12.75 ui
Amplitude Resolution	
"FAST" Scroll	0.5 ui increment/decrement
"SLOW" Scroll	0.05 ui increment/decrement
Amplitude Accuracy	± 5% ± .05 ui
Frequency Range	10Hz to 40kHz
Frequency Accuracy	± 50 ppm
Frequency Resolution	
"FAST" Scroll (Expand enabled)	106 LOG spaced increments
"SLOW" Scroll (Expand enabled)	>1600 LOG spaced increments

2.1 OPTION HIGHLIGHTS

The JO2 option permits the user to perform the following jitter tests of T-1 equipment and/or facilities:

Measure Jitter

- ¤ Total wideband (10Hz to 40kHz) Jitter Amplitude (to 13 Unit Intervals)
  - ° Peak to Peak unit intervals, or
  - ° Negative peak unit intervals, or
  - ° Positive peak unit intervals.
- ¤ Jitter Spectrum Analysis
  - ° Automatic sweep, 10Hz to 40kHz in 106 LOG steps.
  - ° Numerical readout and easily interpreted graphic display for each of 106 spectral measureaments.
  - ° AT&T jitter specification limit mask displayed with numeric readout.
  - ° Automatic identification of out-of-specification measurements.
  - ° Optional manual control of narrowband spectral measurements.
- ¤ Jitter Measurement Flexibility
  - ° Framed T1
  - ° Unframed T1
  - ° Live traffic, bridged or terminated
  - ° Remote Control

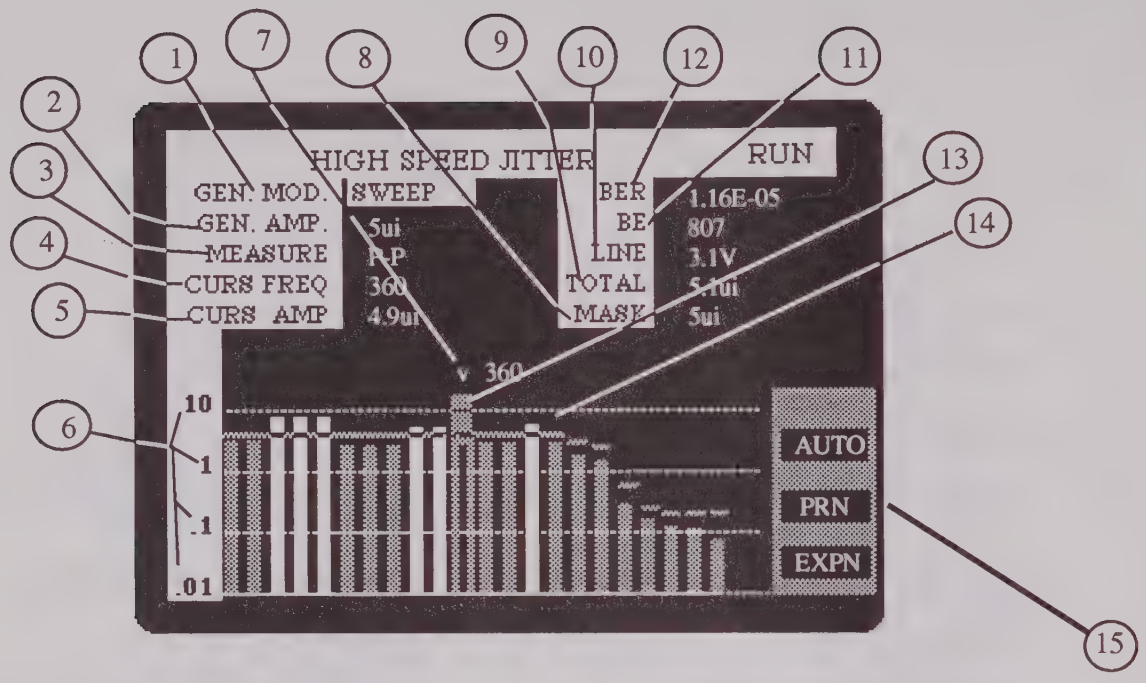
Inject Jitter

- ¤ Sweep AT&T Specification Limit Mask
  - ° Automatic sine sweep, 10Hz to 40kHz, in 106 LOG steps.
  - ° Numeric readout of injected amplitude unit intervals and frequency.
  - ° Simultaneous measurement of received jitter, bit errors, etc.
  - ° Choice of any Model 5500 BERT patterns (QRW is AT&T standard).
  - ° Optional manual control of all jitter injection parameters.
    - * Sine wave or triangle modulation
    - * 1600 step frequency resolution (fast/slow cursor frequency control)
    - * .05 unit interval amplitude resolution (fast/slow scroll)
    - * 12.75 unit intervals maximum
- ¤ Jitter Injection Flexibility
  - ° Framed T1 (D4)
  - ° Unframed T1
  - ° AMI or B8ZS
  - ° Analog modulation input
  - ° Remote control

3.0 OPERATION

3.1 CONTROLS AND INDICATORS

Figure 3-1 presents the 5500 Display and Controls with the JO2 option installed. Table 3-1, which is keyed to figure 3-1, provides a detailed description of the functions of the various display items and softkey controls.



15 SoftKeys are redefined as a function of selected GEN. MOD. operating modes

GEN. MOD.
SWEEP

AUTO	Enables auto sweep of jitter tolerance mask.
PRN	Activate to print out a bar graph of the entire measured jitter display graph
EXPN	Compressed display mode.
MAN.	Enables manual control of CURS FREQ with interlocked auto AMP control.
	Indicates Printer Port not enabled.
EXPN	Enables high resolution display mode (1/5 of total spectrum displayed).

GEN. MOD.
SIN
TRI
OPT
OFF

FAST	Enables coarse CURS FREQ resolution and coarse GEN. AMP. resolution.
PRN	Activate to print out a bar graph of the entire measured jitter display graph.
EXPN	Compressed display mode.
SLOW	Enables fine CURS FREQ resolution and fine GEN. AMP. resolution.
	Indicates Printer Port not enabled.
EXPN	Enables high resolution display mode (1/5 of total spectrum displayed).

Figure 3-1. 5500 Display and Controls

Table 3-1 Model 5500-JO2 Controls and Indicators

INDEX NUMBER	DISPLAY	FUNCTION
1	GEN. MOD.	GENERATOR MODULATION, selects the type of Jitter modulation to be injected in the transmit jitter clock (note: Jitter modulation of the transmit data requires selection of CLOCK SOURCE = JIT CLK on the BERT FORMAT MENU). SWEEP, SIN, TRI, OPT and OFF are the selection options.
1a	GEN. MOD.	**SWEEP** - automatically sweeps the AT&T jitter tolerance mask per figure 14 of Bell System Technical Reference PUB62411. The frequency of the JIT CLK sinusoidal modulation is automatically swept from 10 HZ to 40 kHZ, while automatically controlling the amplitude of the JIT CLK modulation to that specified by the AT&T jitter tolerance mask: 10 HZ to 500 HZ = 5 ui (unit intervals) 500 HZ to 8 KHZ = -8.5 dB/Octave to 0.1 ui @ 8 KHZ 8 KHZ to 40 KHZ = 0.1 ui The SWEEP may be halted at any point by activating the AUTO softkey to MAN. When in the SWEEP MAN mode, the CURS FREQ may be manually adjusted via the SELECT key (the GEN. AMP. will automatically track the AT&T mask). When the AUTO/MAN soft key is cycled from AUTO to MAN and back to AUTO, the direction of the sweep will be reversed. Resolution of the GEN. AMP. control is .05 ui, and the GEN. AMP. will automatically be set to the .05 ui increment closest to the actual MASK limit at the CURS FREQ (CURSOR FREQUENCY). The actual MASK limit is displayed (5th parameter down on right side) to two significant decimal places.
1b	GEN. MOD.	**SIN** - Selects Sinewave Jitter Modulation. The amplitude of the sinewave modulation is controlled by scrolling the GEN. AMP. with the SELECT Key. In this mode, the amplitude of the jitter moduation is not forced to the AT&T spec limit, and the jitter moduation may be adjusted from 0 ui to 12.75 ui in .05 ui steps (FAST/SLOW soft key = SLOW). Note that the functions of the three soft keys (at the lower right side of the CRT) are redefined when the GEN. MOD. mode is changed from SWEEP to one of the four alternate modes (see figure 3).
1c	GEN. MOD.	**TRI** - Selects Triangle wave Jitter Modulation. The peak-to-peak amplitude of the triangle wave jitter modulation is controlled the same as for sinewave modulation. The modulation wave form is a 50% duty cycle linear triangle function having odd harmonic content decreasing at 12 dB per octave.
1d	GEN. MOD.	**OPT** - Selects an OPTIONAL Jitter Modulation Waveform. The jitter waveforms are specified by a PROM memory device with 100 points per period below 15 KHZ, and 16 points per period above 15 KHZ. One section of the PROM is allocated for an optional modulation waveform. (A unique waveform may be specified by the user. A one time charge is required. Consult Phoenix customer service for delivery and price.) The OPT waveform in unmodified production hardware is a 50% duty cycle square wave.

Table 3-1 Model 5500-JO2 Controls and Indicators (Cont.)

INDEX NUMBER	DISPLAY	FUNCTION
2	GEN. AMP.	GENERATOR AMPLITUDE, displays the amplitude of the jitter modulation in unit intervals (ui) peak to peak. This is the magnitude of jitter being injected in the transmitter data at the model 5500 T1 TX output jack. In the GEN. MOD. SWEEP mode, this amplitude is automatically set to the level defined by the AT&T jitter tolerance MASK limit (to the closest .05 ui increment) at the selected CURS FREQ. In the GEN. MOD. SIN, TRI or OPT modes, this amplitude is adjustable via the SELECT key from 0 ui to 12.75 ui in .05 ui steps (FAST/SLOW soft key = SLOW) or in 0.5 ui steps (FAST/SLOW soft key = FAST).
3	MEASURE	Displays the selected jitter measurement mode: P - P Peak to Peak jitter amplitude +P average to positive peak jitter amplitude -P average to negative peak jitter amplitude (CURS AMP (#5) and TOTAL (#9) are P-P, +P, -P as indicated above.)
4	CURS FREQ	CURSOR FREQUENCY, displays the frequency of the generator jitter modulation in the GEN. MOD. SWEEP SIN TRI or OPT modes; and displays the selected measurement frequency when the GEN. MOD. is OFF . The CURS FREQ is indicated on the GRAPH display by the tall (off scale high), wide bar (see item 13 on figure 3). The CURS FREQ is adjustable via the SELECT key over the range of 10 HZ to 40 KHZ. The frequency increments and graph scale are approximately logrithmic. Frequency selection resolution varies depending upon the combination of FAST/SLOW and EXPN (EXPAND) mode selections. All automatic SWEEP measurements are made with approximately 10% frequency increments (i.e. 10, 11, 12, 13 ... 20, 22, 24, ... etc.). When the EXPN function is disabled, the graph data is condensed to fit all data from 10 KZ to 40 KHZ onto the CRT screen. The data continues to be obtained at the frequency resolution of the "EXPANDED" mode; however the data is compressed by displaying the highest measured jitter amplitude for 5 contiguous frequency increments as one bar at a single frequency. That is, the EXPN disabled mode results in a 5 to 1 compression of the graph data. This compression is only for the purpose of condensing the data for 106 discrete measurements to be displayed as 22 data points on one screen. All measurement sweeps are performed at 106 discrete frequency increments, all of which may be displayed by scrolling the CURS FREQ in the EXPN mode. No data is lost by switching between the compressed screen and the expanded screen modes - all graph data is retained in memory in the high resolution mode (106 discrete frequency data points). The FAST/SLOW soft key in the SLOW mode results in a frequency resolution of 1/16th that of the FAST mode (i.e. 10, 10.0625, 10.125, ..., 20, 20.125, 20.25, ... etc.), for a resolution step increment of less than 1% in the EXPN SLOW mode of CURS FREQ selection.
5	CURS AMP	CURSOR AMPLITUDE, displays the amplitude of the measured jitter of the received data at the CURS FREQ. This is a narrow band measurement (1/3 octave filter bandwidth) and is given in unit intervals, (ui).

Table 3-1 Model 5500-JO2 Controls and Indicators (Cont.)

INDEX NUMBER	DISPLAY	FUNCTION
6	GRAPH VERTICAL SCALE	The vertical scale for the graph display is logrithmic with greater than three decades dynamic range (>60dB). The display range is from .01 unit intervals to 12.75 unit intervals with horizontal dashed lines identifying the .01, .1, 1 and 10 unit interval amplitudes.
7	v360	The "v" character identifies the graph bar corresponding to the narrow band measurement currently being processed. The measurement frequency is displayed just to the right as in "v 360". In the jitter measurement only mode, when jitter injection is disabled (GEN. MOD. = OFF), continuous readout of a single frequency spectral amplitude is provided via the CURS FREQ and CURS AMP displays, and simultaneously the spectrum analyzer sweeps the displayed frequency band and continuously updates the amplitudes of the measured spectral components. The "v" character (followed by numeric display of frequency) all move from left to right indicating the measurement in progress. With the EXPN function disabled, all 106 measurements will be updated, but the display will be compressed by a factor of 5 to 1. The high resolution results of the complete spectral sweeps may be displayed at any time by activating the EXPN to enable and using the CURS FREQ control to move to the desired area of the spectrum. However, once in the EXPN enabled mode the continuous sweep update of the spectrum is limited to that portion of the spectrum currently displayed (as is clearly indicated by the "v" character and trailing frequency readout).
8	MASK	The amplitude of the AT&T jitter tolerance MASK limit at the CURS FREQ is displayed in unit intervals (ui). This readout is automatically updated to track the selected cursor frequency. This data point is provided as reference data for assessing performance margins at individual frequencies across the spectrum from 10 HZ to 40 KHZ.
9	TOTAL	The amplitude of the wideband jitter amplitude, including all frequency components between 10 HZ and 40 KHZ, is continuously measured and displayed as TOTAL unit intervals of jitter. This measurements is P-P (peak to peak), +P (positive peak), or -P (negative peak) as selected and indicated by the item 3. MEASURE mode.
10	LINE	The approximate amplitude of the bipolar waveform at the RX jacks of the model 5500 T1 module is displayed in volts, average to peak. This measurement is obtained by digitizing the AGC (Automatic Gain Control) voltage level of the Automatic Line Build Out (ALBO) in the line receiver circuit. A software calibration curve converts this measurement to the corresponding line voltage amplitude.
11	BE	BIT ERRORS, displays the number of bit errors measured by the Model 5500 Analyzer. This is one of two programmable parameter display blocks on the high speed jitter menu screen. Any of the greater than 2 dozen available parameter blocks may be selected for display in this position.

Table 3-1 Model 5500-JO2 Controls and Indicators (Cont.)

INDEX NUMBER	DISPLAY	FUNCTION
12	BER	BIT ERROR RATE, displays the measured bit error rate. This is one of two programmable parameter display blocks. The CURSOR positioning and SELECT keys are used to scroll through all available display parameters in each position.
13		The tall, wide bright bar is the cursor bar which highlights the measurement in progress at the selected CURS FREQ. Note that the amplitude of the cursor frequency measurement is indicated by a dark inverse video bar within the bright cursor bar.
14		This stair-stepped line is the Graph of the AT&T Jitter Tolerance limit MASK.
15	SOFT KEYS	As indicated in the chart below the display screen of figure 3, the soft key functions are re-defined for different measurement modes. ° The AUTO/MAN soft key controls the frequency sweeps of the jitter generator in the GEN. MOD. SWEEP mode. This soft key becomes the FAST/SLOW control for both frequency and amplitude in all other modes. ° The PRN function will not be available on this menu if the printer port is not enabled on the Remote Port Set Up Menu. ° See items 1 and 7 for explanation of the interactions of AUTO/MAN and EXPN soft keys.

3.2 THEORY OF OPERATION

The JO2 Option consists of two independent hardware subsections: (A) Jitter Measurement circuitry and (B) Jitter Injection circuitry. The jitter measurement and jitter injection functions may be used interactively or independently as the situation requires.

3.2.1 Theory of Operation - Jitter Measurement

A block diagram of the Jitter Measurement circuitry is shown in figure 3-2. The phase of the received clock (RCV CLK) from the T1 Interface Board is measured against the phase of the long term average of the received clock (AVG RCV CLK) by an analog phase comparator. Both clocks are divided by 16, before phase comparison, to allow detection of phase jitter of greater than 10 unit intervals peak to peak. The RCV CLK LONG TERM AVERAGER consists of a crystal controlled VCO/Phase Lock Loop with a low pass loop filter that allows the VCO to lock to the long term average of the RCV CLK without transferring the RCV CLK phase jitter components (above 10 HZ) to the AVG RCV CLK reference signal for the phase comparator. The analog output of the phase comparator represents the demodulated phase jitter of the RCV CLK (above 10 HZ). This phase comparator output is band limited by a two pole high pass/8 pole low pass filter for the frequency band of interest: 10 HZ to 40 KHZ. This band limited analog demod phase jitter signal is accessible at the phase jitter receive monitor BNC connector (PHASE JITTER RX MON) on the rear of the Model 5500-624 interface module.

Two tuneable solid state 1/3 octave filters are used to perform the spectrum analysis of the receive clock phase jitter demodulation signal: (A) a transversal filter covers the band from 15 KHZ to 40 KHZ, and (B) a switched capacitor filter covers the band from 10 HZ to 15 KHZ. The 2 pole high pass/8 pole low pass filter provides anti aliasing band limiting for the transversal filter; and a separate low band ANTI ALIAS FILTER network (actually a 2 pole low pass active filter with 4 selectable break points) performs anti aliasing for the low band switched capacitor filter. A frequency synthesizer sets the tuned cented frequency of the digital filters by controlling the filter clock drive frequency. The outputs of these two filters are selected through a variable gain network for peak detection. The amplitude of positive peak, negative peak, or peak to peak phase jitter for both the "total" (10 HZ to 40 KHZ band width) and the selected narrow band frequency is then digitized by an analog to digital converter (ADC) and made available to the data bus. Auto ranging of the gain selection, ADC sampling intervals, filter and peak detector dwell times, narrow band filter tuning and other special timing and control signals relating to the dynamics of the spectrum analyzer function are implemented by software control loops via the bi-directional data bus interface. The automatic line build out (ALBO) level from the T1 line receiver circuit is also digitized by the ADC to provide an indication of the received bipolar signal amplitude. This d.c. level is proportional to the gain required to equalize (gain and phase compensate) the received waveform, and a software calibration curve converts the ALBO voltage measurement to the corresponding peak amplitude of the bipolar waveform (3.0 volts peak is nominal).

3.2.2 Theory of Operation - Jitter Injection

A block diagram of the Jitter Injection circuitry is shown in figure 3-3. The Model 5500 analyzer provides a 1.544 MHZ crystal oscillator clock which the JO2 jitter option board uses as a reference clock for the phase jitter modulator. This reference clock is divided by 20, and the output of the jitter modulator VCO is also divided by 20 to allow phase modulation magnitudes in excess of 13 unit intervals. The two divided-by-20 clocks are input to a digital phase comparator which generates a pulse width modulated error signal. The error signal is low pass filtered and applied to one of the VCO control voltage inputs to establish VCO frequency and phase lock to the reference 1.544 MHZ clock. A digital waveform synthesizer, consisting of a Frequency Synthesizer, a Waveform PROM (Programmable Read Only Memory), a Modulation DAC (Digital to Analog Converter), a Gain DAC, and an Accentuation filter generates a modulation waveform for application to the VCO voltage control network. The Waveform PROM defines the modulation waveform amplitude for one complete cycle (or period) with a resolution of 100 points per cycle below 15 KHZ, and 16 points per cycle at 15 KHZ and higher.

The JO2 Waveform PROM defines a Sinewave and a Triangle Wave (50% duty cycle, linear); and includes provisions for a third OPTIONAL waveform. The standard production hardware is delivered with a 50% duty cycle square wave in the "OPT" section of the PROM. (Custom programming of the third "OPT" waveform is available for a one time charge.)

Amplitude and frequency of the injected phase jitter modulation is software controlled via the data bus. The resulting JITTERED CLK is menu selectable for use as the transmit clock source for the Bit Error Rate test patterns generated by the Model 5500. The phase jittered logic data sequences are than encoded into AMI or B8ZS, framed or unframed bipolar signals for transmission on standard T1 digital communication networks.

An external analog phase jitter modulation input connector is accessible at the rear of the Model 5500-624 I/O module. The BNC connector is labeled PHASE JITTER TX INJ. Connection of a general purpose

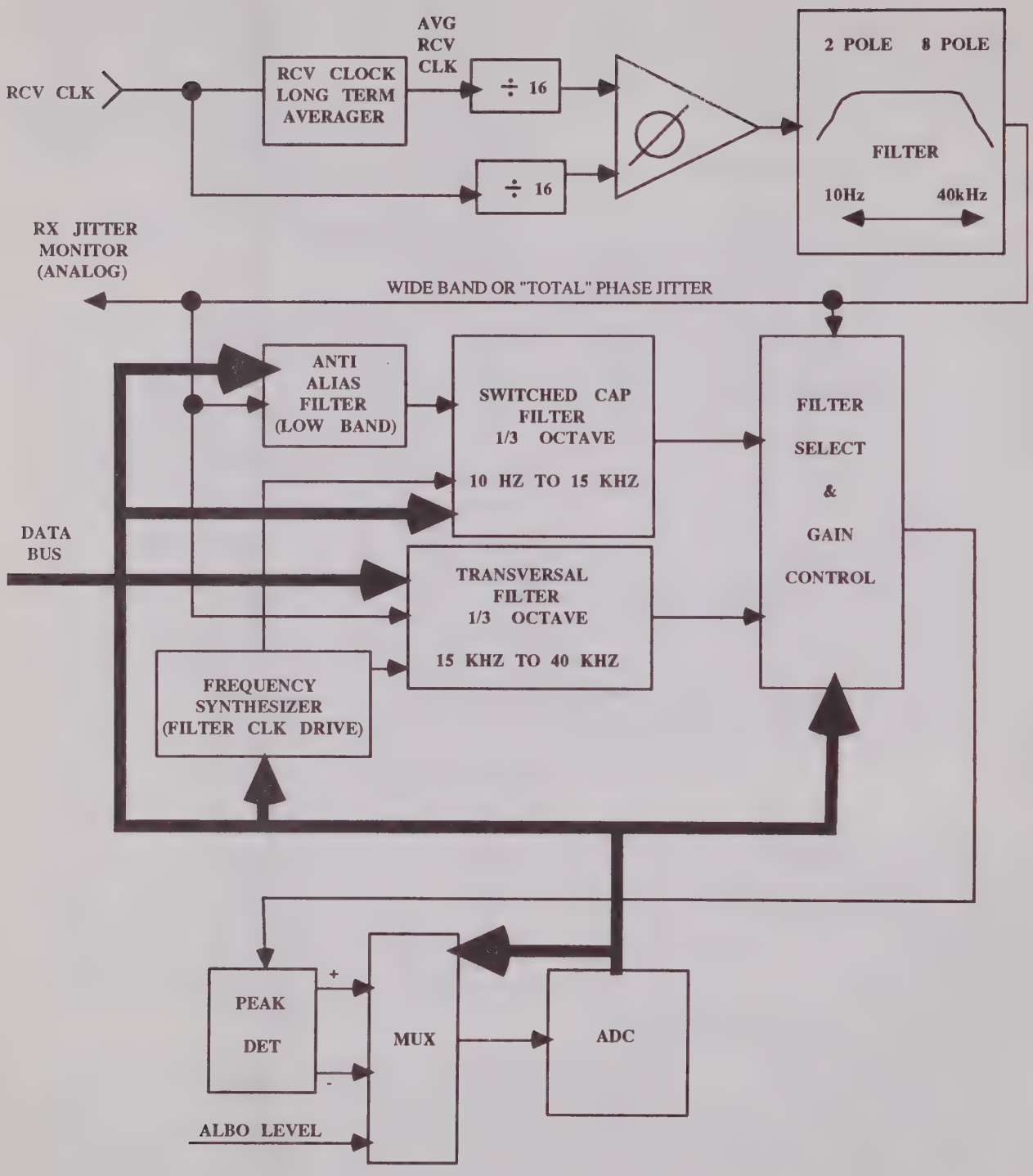


Figure 3-2. Jitter Measurement Block Diagram

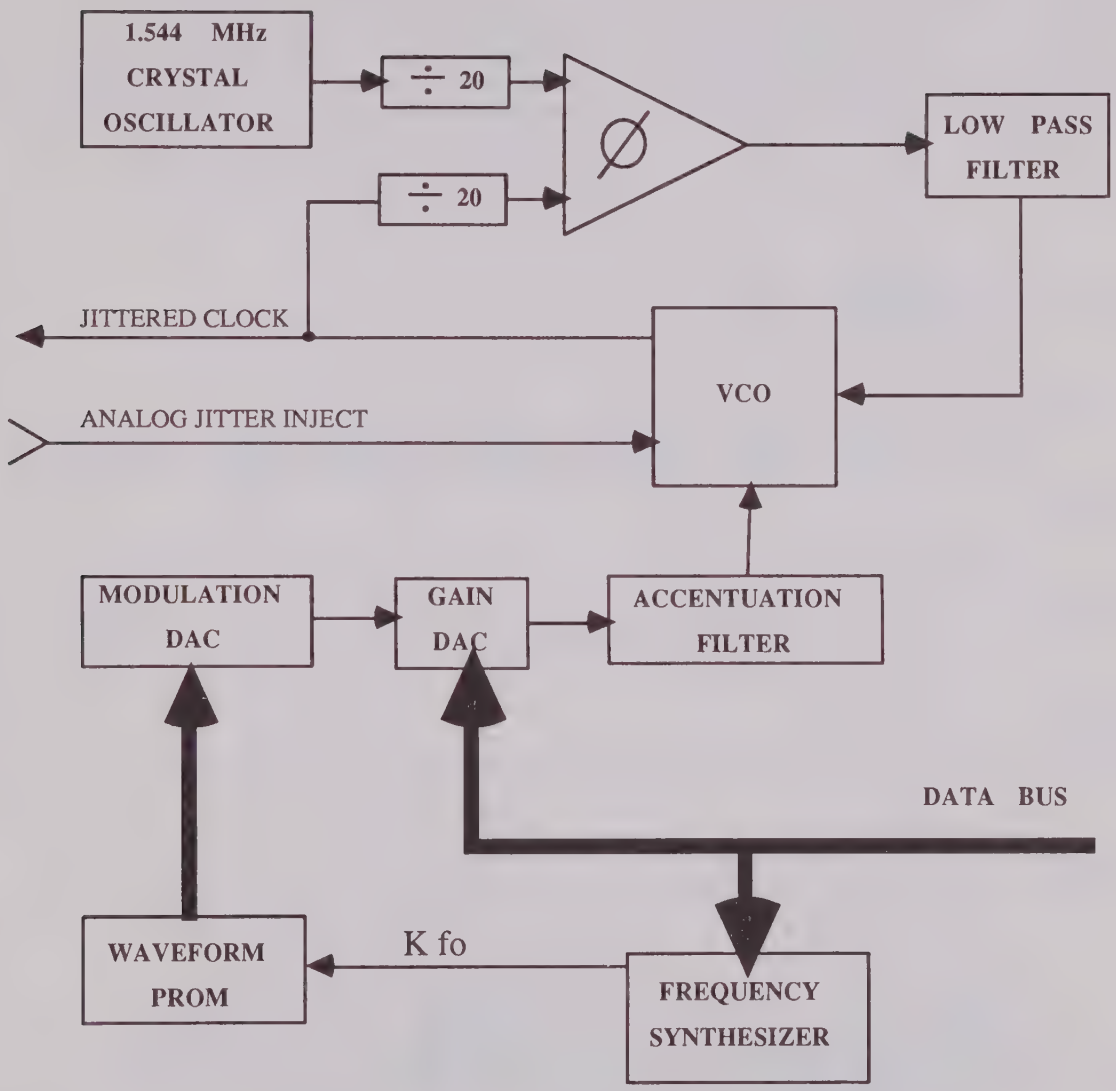


Figure 3-3. Jitter Injection Block Diagram

waveform generator allows external control of phase jitter modulation amplitude and frequency. The JO2 phase jitter measurement features should be used (with the 5500 in "LOOP" mode) to calibrate the external modulation signal. This is accomplished by simply adjusting the amplitude and frequency of the external modulation signal to achieve the desired phase jitter. The external modulation will be superimposed with the selected internal modulation. The use of complex waveforms, random noise, etc. is perfectly acceptable. In fact, the Phoenix JO2 option has been used to successfully phase modulate and demodulate voice communications over the 1.544 MHZ data circuit.

3.3 ILLUSTRATIONS OF T1 PHASE JITTER

Figures 3-4 and 3-5 illustrate two examples of phase jitter as it would appear on the T1 bipolar waveforms as observed via an oscilloscope synchronized to the originating, stable, non-jittered timing source (1.544 MHZ). Two primary causes of phase jitter are (1) frequency offset of span line repeater clock recovery tuned circuits, and (2) phase modulation in the clock recovery/regeneration circuits of multiplexers and de-multiplexers which necessarily must deal with phase jitter associated with the use of stuff bits and/or elastic stores employed to achieve network synchronization.

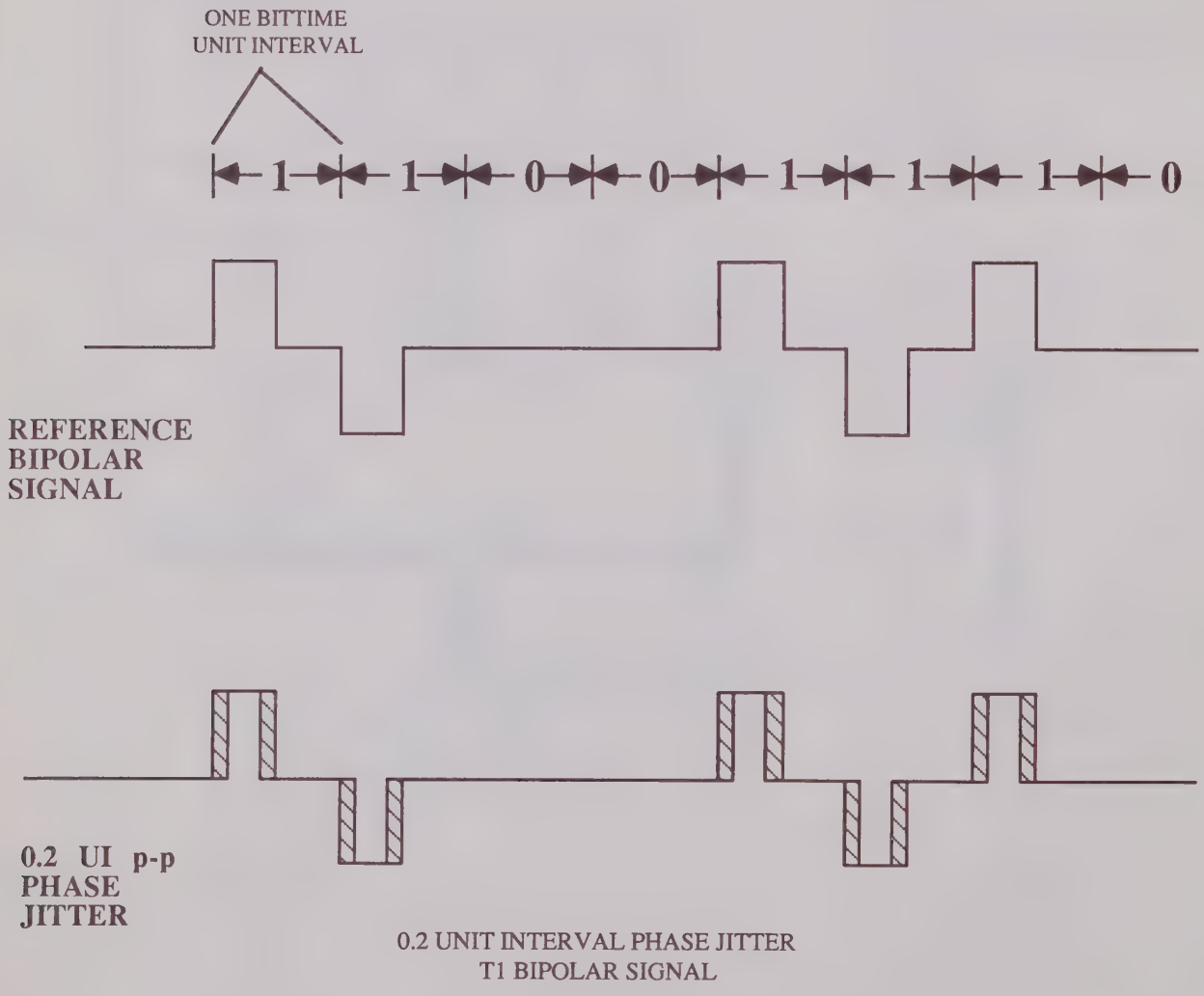
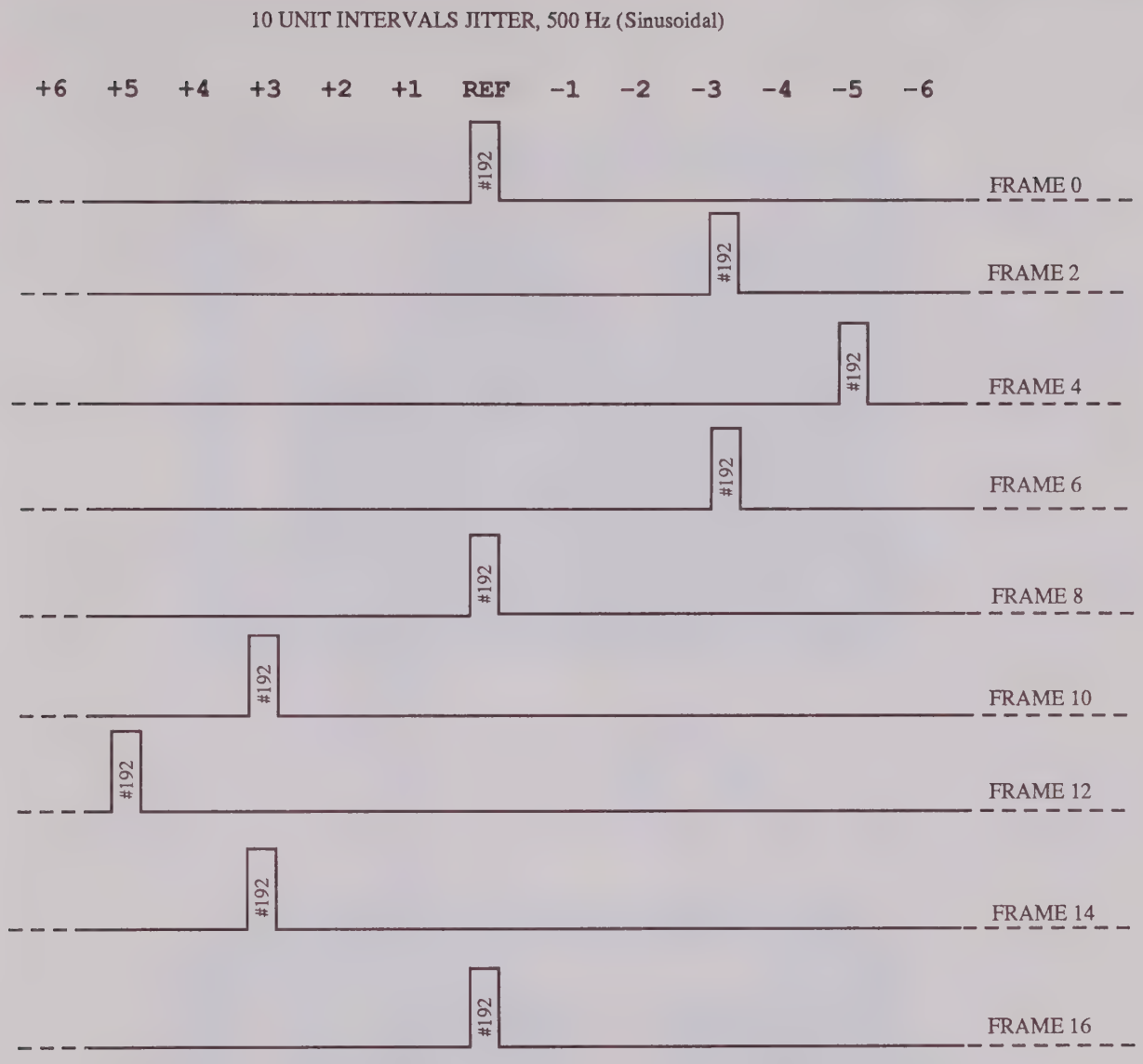


Figure 3-4. Phase Jitter on T! Bipolar Signal



$$\frac{\text{FRAME RATE}}{\text{JITTER FREQUENCY}} = \frac{\text{8000 FRAMES/SEC}}{\text{500 CYCLYES /SEC}} = \text{16 FRAMES/JITTER CYCLE}$$

@ 500 HZ JITTER FREQUENCY

Isolated T1 bipolar pulse No. 192
T1 Frame rate 8000 Hz
193 bits/frame

Figure 3-5. Isolated Pulse Jitter Representation

4.0 JO2 APPLICATION

The following paragraphs provide test set up procedures and examples for using the Model 5500-JO2 high speed jitter option.

4.1 Measure Jitter, Live Traffic, Framed or Unframed

Phase Jitter of a T1 bipolar digital data line may be measured with the JO 2 option, regardless of the transmitted data pattern (LIVE Traffic, BERT PATTERN, KEEP ALIVE SIGNAL, YELLOW ALARM,... D4 FRAMED or NOT D4 FRAMED). When the T1 bipolar signal is connected to the RX Input jack on the rear of the Model 624 interface module, the JO2 option card will recover clock, establish a long term frequency and phase average reference clock, and measure the amplitude and frequency spectra of the received clock phase jitter. This measurement may be accomplished in either the BRDG (Bridged) mode or the TERM (Terminated) mode. For "LIVE" traffic, the Model 5500 analyzer will not achieve SYNC (pattern synchronization) because a known pseudo random test pattern will not be present. Likewise, BE (Bit Error) , BLKE (Block Errors), etc. will not be detected. However, if trouble is reported or suspected on an in service T1 line, the line may be tested for FRAME errors, B2 alarm status, S Bit errors, BPV's (Bipolar Violations), line level and phase jitter without interrupting or interferring with the live T1 traffic. The following set-up procedure will accomplish testing of T1 live traffic:

A) On the Framed T1 FORMAT Menu:

1. Select FRAME [ENABLE]
2. Activate [BRDG] or [TERM] softkey as desired.
3. De-Activate [LOOP]

B) On the HIGH SPEED JITTER menu:

1. Select [GEN.MOD.] = Off
2. Select [GEN.AMP.] = O ui
3. Select [MEASURE] = P-P
4. On the upper right side of this menu there are 2 programmable parameter blocks. Using the CURSOR control keys and the SELECT key, select any 2 test parameters for display, for example:

RBPV	Ø	Received Bipolar Violations
ALRM	. . . . . S . F	The "F" would indicate FRAME errors, the "S" would indicate S - Bit errors.
ALRM	. . . . .	If all Framing bits are correct, the ALRM parameter will be a row of dots.

5. Observe the [TOTAL] jitter amplitude. This is a measure of the total wideband (10HZ to 40KHZ) peak-to-peak jitter amplitude in unit intervals (ui).
6. To determine whether the measured TOTAL jitter is above or below allowable limits, observe the graph display of jitter amplitude for each of 106 narrow band measurements. Any spectral components above the AT&T MASK limit will be highlighted as a bright magnitude bar. Using the CURS FREQ (CURSOR FREQUENCY) control move the graph cursor (tall, wide bar) to coincide with any detected spectral component and observe the numeric amplitude readout beside CURS AMP (CURSOR AMPLITUDE). Compare this number to the MASK value which identifies the numeric limit at the CURS FREQ.
7. An example of a phase jitter measurement is illustrated in figures 4-1 and 4-2. In Figure 4-1, the EXPAND function is disabled and the entire spectrum from 10HZ to 40 KHZ is displayed. In this mode each bar actually represents the results of 5 discrete spectral tests - with the highest jitter measurement in the band of 5 frequencies determining the height of the bar for that group of measurements. This compressed display mode quickly identifies the approximate frequency of any out-of-limits spectral components anywhere in the specified band width. By enabling the [EXPN] function, and adjusting the graph cursor position (by scrolling the CURS FREQ), the high resolution graph mode (as illustrated in fig 4-2) reveals that the measured jitter (for this example) is concentrated at two frequencies. The two frequencies and the amplitudes at each frequency are determined by moving the cursor to each peak and observing the CURS FREQ and CURS AMP numeric readouts.

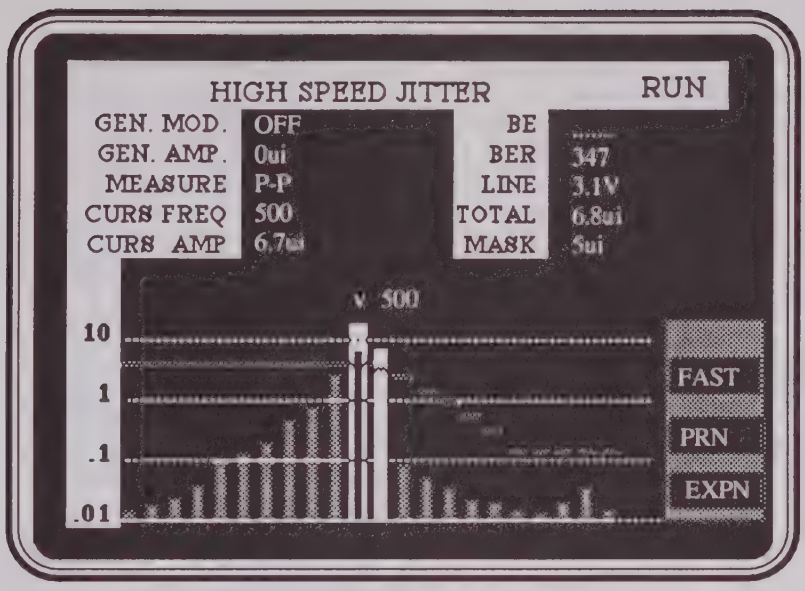


Figure 4-1. Phase Jitter Measurement
Expand Function Disabled

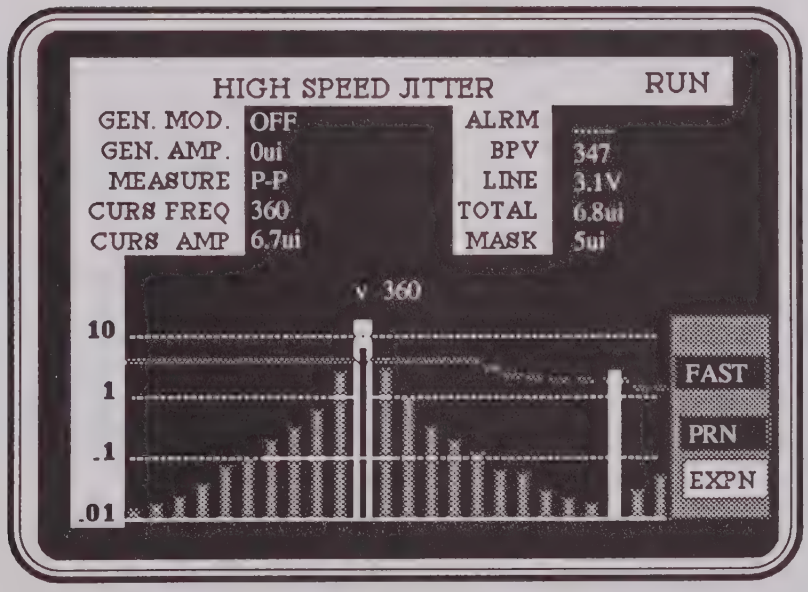


Figure 4-2. Phase Jitter Measurement
Expand Function Enabled

In addition, notice that the "v" character (followed by a number) continues to scroll across the screen above the bar graph as the graph data is continuously updated with new measurements. The number after the "v" indicates the frequency at which the current measurement update is being performed (i.e. "v 330" would indicate a measurement at 330HZ and the bar graph directly below the "v" represents the amplitude of the spectral component at that frequency. In the EXPAND mode, only that portion of the spectrum on the screen (approximately 1/5th of the 10HZ to 40 KHZ spectrum) is continuously updated, as indicated by the movement of the "v" character. When the EXPAND mode is disabled, the entire spectrum is updated - but remember that each bar represents the results of 5 individual spectral measurements. 106 spectral measure-ments are made in one complete sweep and these are compressed into 22 lines with EXPN disabled. The data is "uncompressed" for high resolution display when EXPN is enabled.

4.1.1 Interpreting the Data

The degree of randomness and the one's density of the digital data sequences transmitted over the measured T1 line will have an effect on the amplitude of the measured spectra due to (A) the tuning errors and dynamic response characteristics of the clock recovery circuits in repeaters, multiplexers, CSU's etc, and (B) the intersymbol modulation associated with the phase distortion which occurs in the T1 cables and in the span line repeaters and Model 5500 receiver ALBO's (Automatic Line Build Outs). The AT&T jitter tolerance spec limits are based on test measurements using the standard Bell System Quasi-Random Test Signal (or Quasi Random Word -"QRW"). This signal has 50% ones density and no strings of zeroes greater than 15 (D4 framed; 14 zeroes max when un-framed). The Model 5500 permits the correlation of phase jitter data with BPV and Frame error data on live traffic and also facilitates the characterization of jitter tolerance and jitter transfer function performance in accordance with the AT&T specifications. Futhermore, the use of USER specified test patterns facilitates testing with worst case one's density (12.5%) and evaluation of clock recovery circuit dynamics and design margins by subjecting the receivers to excessively long strings of zeros with varying degrees of one's density.

4.2 Inject Jitter, Evaluate Jitter Tolerance

When measuring jitter tolerance of a T1 facility or span line or its component parts such as repeaters, multiplexers, CSU's and Bit Error Rate Testers! (the test sets need to be better than the facilities they are testing!), the object is to stress the system with phase jitter modulation of the data transmitted into the facilities (or component parts) and observe the ability of the facilities to transport the data without incurring unacceptable levels of bit errors, sync losses, framing errors, etc. The Model 5500 Analyzer with Model 624 Framed T1 module and JO2 High Speed Jitter option provides the capability to inject a controlled phase modulation onto a standard T1 bipolar interface signal. The amplitude and frequency of the phase modulation may be controlled to determine the threshold of susceptibility to phase jitter over the phase modulation frequency range of 10HZ to 40 KHZ. The GEN.MOD. SWEEP mode provides for an automatic sweep of the AT&T jitter tolerance mask (per PUB 62411, figure 14). In this mode, phase jitter modulation at the MASK level is injected at each of 106 frequencies (at one frequency at a time) logarithmically spaced across the spectrum at approximately +10% increments. As the jitter modulation sweep is continuously repeated, the Model 5500 performs a continuous bit error test of the bipolar T1 signal transported through the facility or equipment under test and returned to the RX input jack of the Model 624 interface module. If bit errors, sync losses, BPV's, framing errors, etc. are detected at a given area of the spectrum, then the GEN.MOD. mode may be switched to the manual SINEwave mode to determine the level of susceptibility at the specific frequencies of interest. In this mode the GEN.AMP. level of phase jitter modulation may be raised or lowered to assess the degree of phase jitter susceptibility (i.e. Bit Error Rate versus modulation level; or threshold of induced errors). The GEN.MOD. mode also allows the use a TRI angle wave modulation (odd harmonic spectral content decreasing at 12dB/Octave). An external analog TX INJ Phase Jitter modulation input allows the use of random noise generators and/or waveform generators to faciltiate testing with more complex phase jitter modulation waveforms.

The following set-up procedure and display examples will illustrate the jitter tolerance test capabilities of the JO-2 option:

A) On the FRAMED T1 FORMAT menu:

1. Select LINE CODE AMI or B8ZS , as required.
2. Select FRAME ENABLE or DISABLE, as required
3. Select PATTERN QRW or other pattern as required.
4. Select BLOCK SIZE 10^6
5. Select BLOCKS 0
6. Set BPV INJ RATE and LOGIC ERR RATE as desired

7. Select CLOCK SOURCE [JIT CLK]

Note: If the phase modulated JITTER CLOCK is not selected as CLOCK SOURCE, the transmitted bipolar signal will not be phase jittered.

8. Select AUTO RESYNC [ENABLE]

9. Set SOFTKEY functions to:

   [BRDG] (Disabled)

   [TERM] (ENABLED) - RX Input Terminated in 100 ohms

   [LOOP] (DISABLED)

B) On the HIGH SPEED JITTER menu:

1. Select [GEN MOD] = SWEEP

2. [GEN AMP] is automatically controlled by the Model 5500 analyzer

3. Select [MEASURE] = P-P

4. [CURS FREQ] is automatically swept from 10 HZ to 40 KHZ in 106 log steps

5. [CURS AMP] will display the amplitude of the measured jitter on the RX input signal. This is a measure of the jitter transfer function which may or may not have direct correlation with the jitter tolerance of the facilities under test. For example, the "Q" of the clock recovery LC tank circuit in a typical repeater will affect the jitter tolerance of the repeater and the jitter attenuation characteristics of the repeater. If the "Q" is relatively "low", the jitter tolerance may be relatively "high" because the jittered clock can quickly pull the phase of the LC tank oscillator to track the phase jitter, resulting in little reduction or attenuation of the phase jitter in the regenerated data. Conversely, if the "Q" is relatively "high", the jitter tolerance may be relatively "low" because the jittered clock cannot quickly pull the phase of the high Q LC tank to track the phase jitter. This high "Q" clock recovery circuit would offer relatively high attenuation of high frequency jitter. That is, high "Q" clock recovery might result in poor jitter tolerance but good jitter attenuation for its limited jitter range; and low "Q" clock recovery might result in good jitter tolerance but very little jitter attenuation (also poor margin for excessively long strings of zeros in the data pattern). The best repeater circuits will either make a compromise of the two parameters or (for more $) use more complex circuitry such as rate buffers, long term averaging clock de-jitter circuits, etc., to optimize both parameters (i.e. high jitter tolerance and removal of all high frequency jitter in the regenerated clock). The point is, the jitter transfer function is a very meaningful parameter but does not necessarily have consistent correlation with jitter tolerance. Jitter transfer function testing is illustrated in the next example (see section 4.3).

6. On the upper right side of the HIGH SPEED JITTER menu there are 2 programmable parameter blocks. Using the CURSOR control keys and the SELECT key, select 2 test parameters for display, for example:

   [BE] Ø

   [BER] Ø

7. In the event errors were induced during initial set up of this test, it may be necessary to clear the BE, BER, etc. test parameter data fields. To reset all error counters to zero, go to the BERT menu and actuate the CLR softkey. Figure 4-3 illustrates the HIGH SPEED JITTER display screen for the SWEEP mode.

8. The jitter sweep will continue from 10 HZ to 40KHZ, and will automatically reverse direction back to 10HZ, and will continue repeating the SWEEP until disabled by the operator. Each SWEEP consists of injecting jitter at the MASK amplitude for each of 106 spectral components from 10HZ to 40KHZ.

9. The BE and BER displays will indicate all detected Bit Errors and the cumulative Bit Error Rate. Framing errors, BPV's, Sync Loss Seconds, Errored Seconds, etc., may also be used in assessing jitter tolerance. The 5500 analyzer will continue to record all error parameters. The "acceptable" levels of the various error conditions are ultimately up to the customers needs and market forces. The Phoenix Model 5500 Analyzers with Model 624 T1 Interface Module and JO2 Jitter Option is required to pass this jitter tolerance SWEEP test, error free, including 24 hours burn-in at elevated temperature. Testing in other than a laboratory

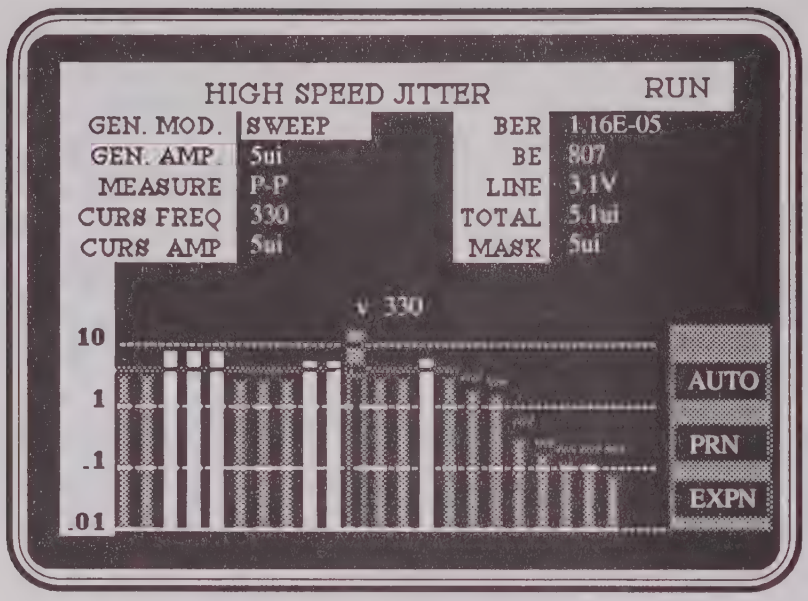


Figure 4-3. High Speed Jitter Display
Sweep Mode

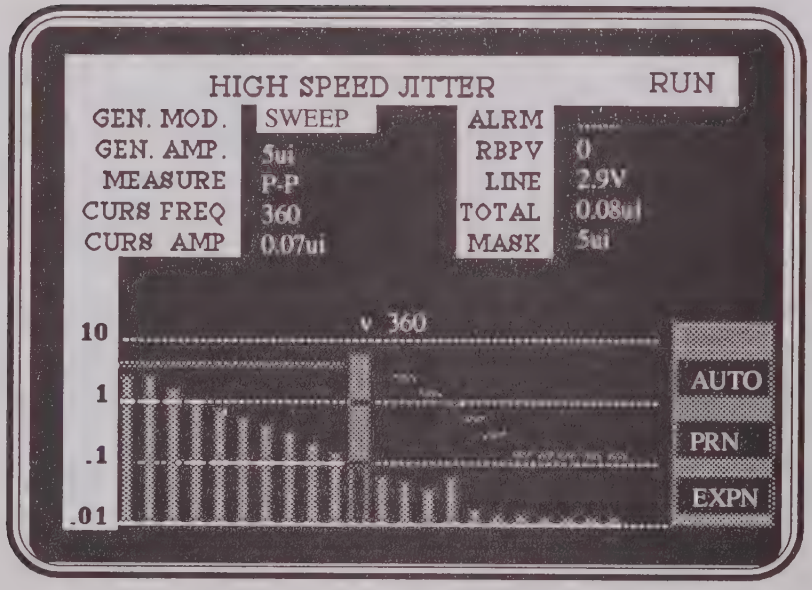


Figure 4-4. High Speed Jitter Display
Jitter Transfer Function

environment and over long haul communications facilities may necessarily require less exacting levels of performance. But in any event, the Phoenix equipment will identify degradations of performance related to phase jitter. The phase jitter graph will display the amplitude of the jitter modulation returned to the 5500 via the RX input jack. And as previously discussed, this data will be an accurate measure of the jitter transfer function, but it may not consistently correlate with jitter tolerance.

10. Select [GEN.MOD.] = SIN To allow manual control of the amplitude and frequency of the injected jitter modulation.

11. Select [CURS FREQ] = 500 500HZ is generally a good "quick look" test point to obtain a relative indication of overall jitter tolerance margins.

12. Increase [GEN.AMP] from 0 ui in 0.5 ui steps, while observing the [BE] parameter block for Bit Errors. Continue adjusting the [GEN.AMP.] up (and/or down as necessary) to find the highest level of jitter modulation that can be tolerated without causing any Bit Errors (or until an acceptable Bit Error Rate is achieved, if you prefer). In some cases, the jitter tolerance of the equipment under test will exhibit hysteresis, requiring the jitter modulation to be lowered considerably before error free operation can be resumed. If the equipment will tolerate 7.5 ui of jitter at 500HZ, where the MASK limit level is 5ui, then the performance margin is 2.5ui or +50%.

13. To completely characterize the jitter tolerance margin over the entire spectrum, step the CURS FREQ and repeat the amplitude adjustment to determine the threshold of Bit Errors or acceptable Bit Error Rate at each frequency of interest.

14. By selecting the [SLOW], [EXPN] mode with the softkeys, the test frequency may be adjusted with high resolution (≅ 0.624% increments) over 1600 discrete test intervals (log spaced) across the 10HZ to 40 KHZ spectrum.

15. The ability to precisely control the frequency of modulation with 1600 step resolution may be especially important in locating the peaking frequencies in an under damped clock recovery network response to the jitter modulation.

4.3 Inject Jitter, Evaluate Jitter Transfer

Performance specifications for CSU's, multiplexers and other T1 interface devices include requirements for attenuation of phase jitter of T1 signals passed through the equipment. In troubleshooting a system or in configuring a new system to accomplish compliance with the network interface requirements, it may be necessary, and certainly advantageous, to select components whose jitter transfer attenuation characteristics compensate or compliment one another (including masking the jitter tolerance problems of downstream equipment) in the system configuration. Evaluation of the jitter transfer function of individual components, as well as the complete system, is therefore beneficial in engineering solutions to jitter compliance problems. The following set up procedure and display example illustrate the use of the Phoenix Model 5500 to measure the phase jitter transfer of T1 equipment and/or complete transmission facilities:

A) On the FRAMED T1 FORMAT menu:

1. Select LINE CODE [AMI] or [B8ZS], as required.
2. Select FRAME [ENABLE] or [DISABLE], as required
3. Select PATTERN [QRW] or other pattern, as desired
4. Select BLOCK SIZE [10^6]
5. Select BLOCKS [0] for continuous test
6. Select CLOCK SOURCE [JIT CLK]

Note: If the phase modulated JITTER CLOCK is not selected as CLOCK SOURCE, the transmitted bipolar signal will not be phase jittered.

7. Select AUTO RESYNC [ENABLE]
8. Set SOFTKEY functions to:

[BRDG] (DISABLED)

[TERM] (ENABLED)

[LOOP] (DISABLED)

B) Connect the equipment or facility under test to the TX output and RX input jacks on the rear of the model 624 interface module with JO2 option.

C) On the HIGH SPEED JITTER menu:

1. Select GEN.MOD. = SWEEP
2. GEN.AMP. level control will be automatic in this mode.
3. Select MEASURE = P-P
4. CURS FREQ contol will be automatic in this mode.
5. CURS AMP will display the level of phase jitter at the RX input, measured at the CURS FREQ, which is the same frequency as the modulation of the jitter clock of the transmitted data at the TX output.
6. The graph will display the amplitude bar graph of the received jitter in comparision to the MASK level of the transmitted jitter. This illustrates the jitter transfer function of the equipment under test. An example is provided in figure 4-4.
7. Numeric readouts of each spectral component may be obtained by commanding a print out of the spectrum graph and data. This data will include the reference MASK level transmitted modulation for each measurement frequency. A sample print out is presented in figure 4-5.
8. At the high end of the spectrum, in the region of 40KHZ, when measuring the level of attenuation of a 0.1 ui injected jitter modulation, the noise floor and resolution limits of the JO2 option may require the use of a higher level injected phase modulation in order to measure attenuation magnitudes as high as 20 dB. For example, if the noise floor of the jitter measurement is 0.02 ui for an injected jitter magnitude of 0.1 ui, then the maximum level of measureable attenuation is $20 \log_{10} .1/.02 = 13.98$dB. By adjusting the GEN.AMP. to 0.2ui in the GEN.MOD. SIN mode, the maximum level of measureable jitter attenuation is increased by 6dB:

$$20 \log_{10} .2/.02 = 20\text{db}$$

9. If greater dynamic range or more precise frequency resolution is required, then a spectrum analyzer can be connected to the RX MON PHASE JITTER connector on the rear of the Model 624 interface module. The output calibration scale factor of the demodulated phase jitter at this connector may be determined by measuring the demod level at a reference amplitude of 5 ui at 500HZ with the Model 5500 in LOOP mode. The amplitude of the measured phase jitter at a given modulation frequency is directly (linearly) proportional to the voltage amplitude of the demod output spectral component at that modulation frequency.

```
JITTER GENERATOR: SWEEP
TOTAL JITTER: 5.1  LINE LEVEL: 2.9V

FREQUENCY   !.01          !.1           !1            !10   AMPLITUDE   MASK
--(HZ)---   !------------!-------------!-------------!---  --(UI)---  -(UI)-
   10     * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5.1        5
   11       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5          5
   12       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.8        5
   13       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.8        5
   14     * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5.1        5
   15     * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5.1        5
   16     * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5.3        5
   17       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.8        5
   18       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.5        5
   19       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.7        5
   20     * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5.3        5
   22     * +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5.4        5
   24       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.7        5
   26       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5          5
   28       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       5          5
   30       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.7        5
   33       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.9        5
   36       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>>>0    !       4.2        5
   39       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>>>> 0    !       3.5        5
   42       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>>   0    !       2.6        5
   46       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>>>    0    !       2.1        5
   50       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>>      0    !       1.6        5
   55       +>>>>>>>>>>>>>+>>>>>>>>>>>>>+>>       0    !       1.31       5
   60       +>>>>>>>>>>>>>+>>>>>>>>>>>>>!         0    !       .91        5
   66       +>>>>>>>>>>>>>+>>>>>>>>>>>>> !        0    !       .72        5
   72       +>>>>>>>>>>>>>+>>>>>>>>>>>   !        0    !       .55        5
   79       +>>>>>>>>>>>>>+>>>>>>>>>     !        0    !       .41        5
   86       +>>>>>>>>>>>>>+>>>>>>>       !        0    !       .32        5
   94       +>>>>>>>>>>>>>+>>>>>>        !        0    !       .26        5
  100       +>>>>>>>>>>>>>+>>            !        0    !       .14        5
  110       +>>>>>>>>>>>>>+>>>           !        0    !       .16        5
  120       +>>>>>>>>>>>>>+>>            !        0    !       .14        5
  130       +>>>>>>>>>>>>>!              !        0    !       .09        5
  140       +>>>>>>>>>>>>>+              !        0    !       .1         5
  150       +>>>>>>>>>>>>>!              !        0    !       .09        5
  160       +>>>>>>>      !              !        0    !       .03        5
  170       +>>>>>>>      !              !        0    !       .03        5
  180       +>>>>>>>      !              !        0    !       .03        5
  190       +             !              !        0    !       .01        5
  200       +>>>>         !              !        0    !       .02        5
  220       +>>>>         !              !        0    !       .02        5
  240       +             !              !        0    !       .01        5
  260       +             !              !        0    !       .01        5
  280       +             !              !        0    !       .01        5
  300       +             !              !        0    !       .01        5
  330       +             !              !        0    !       .01        5
  360       +             !              !        0    !       .01        5
  390       +             !              !        0    !       .01        5
  420       +             !              !        0   1       .01        5
  460       +             !              !        0    !       .01        5
  500       +>>>>         !              !        0    !       .02        5
  550       +             !              !       0     !       .01        4.37
```

Figure 4-5. Sample Graph Printout
Sheet 1 of 2

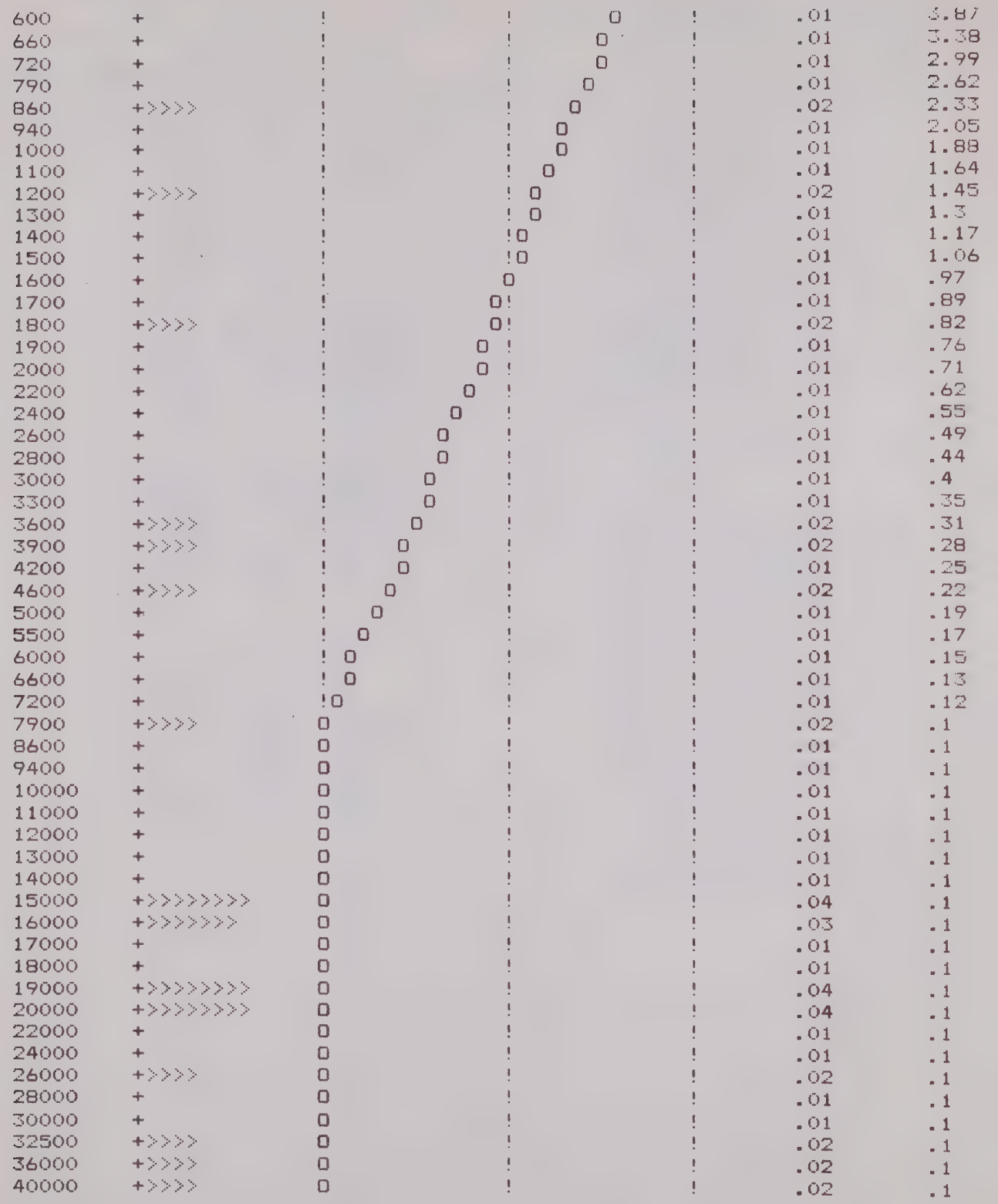


Figure 4-5. Sample Graph Printout
Sheet 2 of 2

Model 5500-700

T-2 Interface Module

1.0 INTRODUCTION

The Model 5500-700 T-2 Interface Module enables the Model 5500 to test T-Carrier Systems operating at 6.312 Mbps rates (T-2) in accordance with the applicable Bell System and U.S. Telephone Association specifications. The module provides two output levels to simulate the 6.312 Mbps signals found at both terminal equipment and at the DSX-2 cross connect, as well as providing the capability to monitor the signal levels originating from both locations. The T-Carrier signals for T-2 are serial, bipolar (return-to-zero) pulses that utilize the Bipolar with six zero substitution (B6ZS) line code. The T-2 Interface Module provides this capability, and in addition, may be configured to provide the Alternate Mark Inversion (AMI) line code via switch selection on the module.

The Model 5500-700 T2 Interface Module enables the Model 5500 to generate and receive T2 serial data streams, recover clock, and regenerate data from low level signals. The mechanical interface between the module and the system under test consists of Western Electric Company type 310 compatible jacks for transmit and receive.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-700 Interface Module.

Table 2-1. Model 5500-700 Specifications

CHARACTERISTIC	SPECIFICATION
TRANSMITTER	
Pulse Rate	T2-6.312 Mbps ±33 ppm
Output Pulse Amplitude (user selectable)	DS2H-2.1V Peak ±10% DSX2-2.1V Peak ±10% in series with a 1000 ft. ABAM cable simulator (LBO)
Output Pulse Shape	DS2H-Rectangular, 78 ±8 nsec pulse width at 50 percent amplitude. DSX2-In accordance with AT&T compatibility bulletin No. 119 DSX2 pulse template.
Overshoot	Less than 10% of amplitude height.
Line Code	B6ZS of AMI (user selectable)
RECEIVER	
Input Level	DS2H - ±2.1v peak plus up to 2155 ft. ABAM cable. DSX2 - .2-7.3 dbm plus up to 1000 ft. ABAM cable.
Input Impedance	110 ohms ±5% terminated. >1000 ohms bridged.

2.1 FUNTIONAL DESCRIPTION

The Generator section (refer to figure 2-1) consists of a line encoder, a line driver, and a series 1000 ft. ABAM cable simulator (LBO) that may be selected via the switch on the T2 Interface Module panel. The LBO is placed in series with the line driver in the "DSX2" switch position. The line encoder can be configured to produce an AMI or B6ZS line code for the bit stream at the T2 rate.

The model 5500 T2 BERT Display and Format Menus (refer to figures 2-2 and 2-3) display the line code. When position 1, SW3, of the T2 Interface Module is in the "ON" position, these display areas will display "B6ZS" or "HDB3". When the switch is in the "OFF" position, these display areas will display "AMI" or B8ZS". Since T2 will only utilize AMI or B6ZS, the proper line code may be selected via the menu soft keys once the switch on the T2 Interface module has been placed in the desired position.

The receive section of the module contains two independent receivers. This configuration enables the Model 5500 to monitor both Receive pair and Transmit pair traffic for Bipolar Violations. The Receive input has a switchable line termination to enable it to receive input signals and terminate them in 110 ohms, as well as monitor signals in a Bridged mode. With the exception of the switchable impedance, each receiver is the same. The receiver section recovers and regenerates the signal at the DSX point or from terminal equipment. The clock recovery circuit (basically a phase locked loop) derives timing from the incoming bit stream and feeds it to the data detector, line decoder, and the Model 5500 internal logic. The Receive Clock and received Transmit Clock are both recovered in this manner.

The Data Detector accepts the output signal of the Receiver and combines it with the recovered clock to do the final reshaping and regeneration of the input which is then passed to the Line Decoder and Bipolar Violation Detector. The Line Decoder is set to AMI or B6ZS as appropriate and converts the line coded signal to a TTL level bit stream for analysis by the Model 5500 internal logic. The BPV detector compares the output of the Data Detector to the AMI coding rule and passes information on violations of the rule to both the line Decoder and Counter Timer circuits which in turn initiate the count of BPV's displayed on the CRT.

In the B6ZS mode of operation the Line Decoder and Bipolar Violation Detector combine to ignore intentional Bipolar Violations.

3.0 OPERATION

Selection of the line code is performed in the following manner:

1) Remove the top cover of the T2 Interface Module, held in place with four Phillips head screws.

2) Carefully separate the top PC board (T2 I/O Module Board) from the bottom PC board (T2 Control Board) and remove the transmit and receive cable connectors from the top PC board.

3) Configure SW3, position 1, for the desired line code. Select "ON" for B6ZS or "OFF" for AMI (refer to figure A below).

4) Reassemble the T2 Interface Module, taking care not to bend any of the pins on the connectors between the top and bottom PC boards.

NOTE: Switch positions other than SW 3, position 1, are shown for illustration **ONLY,** and may or may not represent the factory setting for your module.

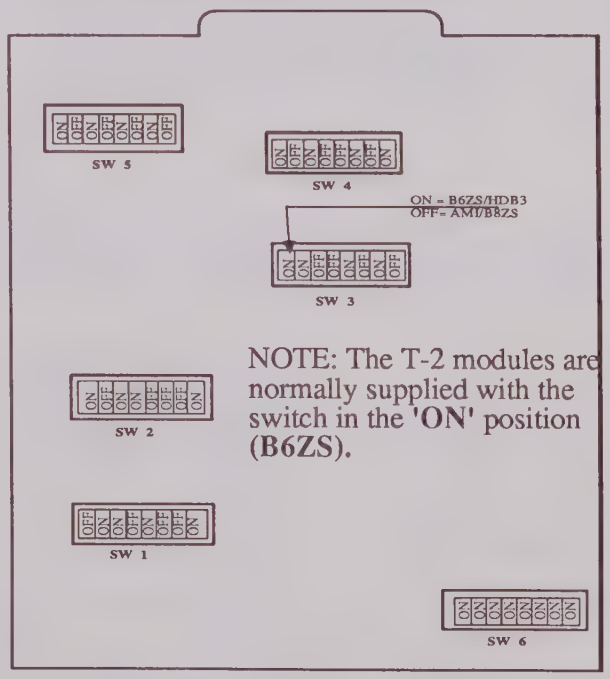


Figure A

3.1 BERT FORMAT DEFINITIONS

Table 3-1 presents the T-Carrier BERT Format definitions that are unique to the Model 5500-700 Interface Module.

3.2 BER TEST ASSISTANCE

Table 3-2 presents a list of possible problem areas if the Model 5500 does not achieve synchronization with the device under test.

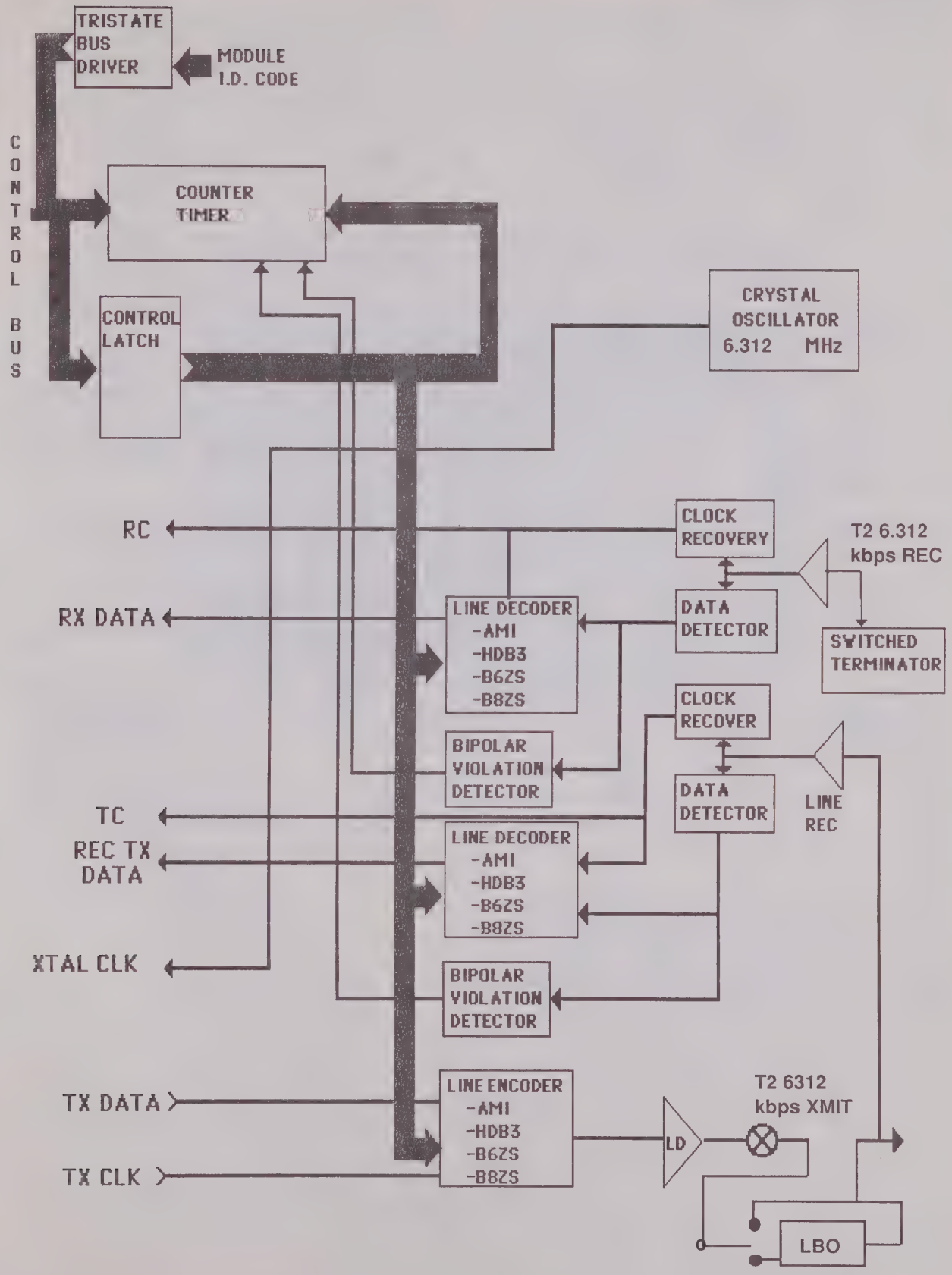


Figure 2-1. Model 5500-700 T-2 Interface Module Block Diagram

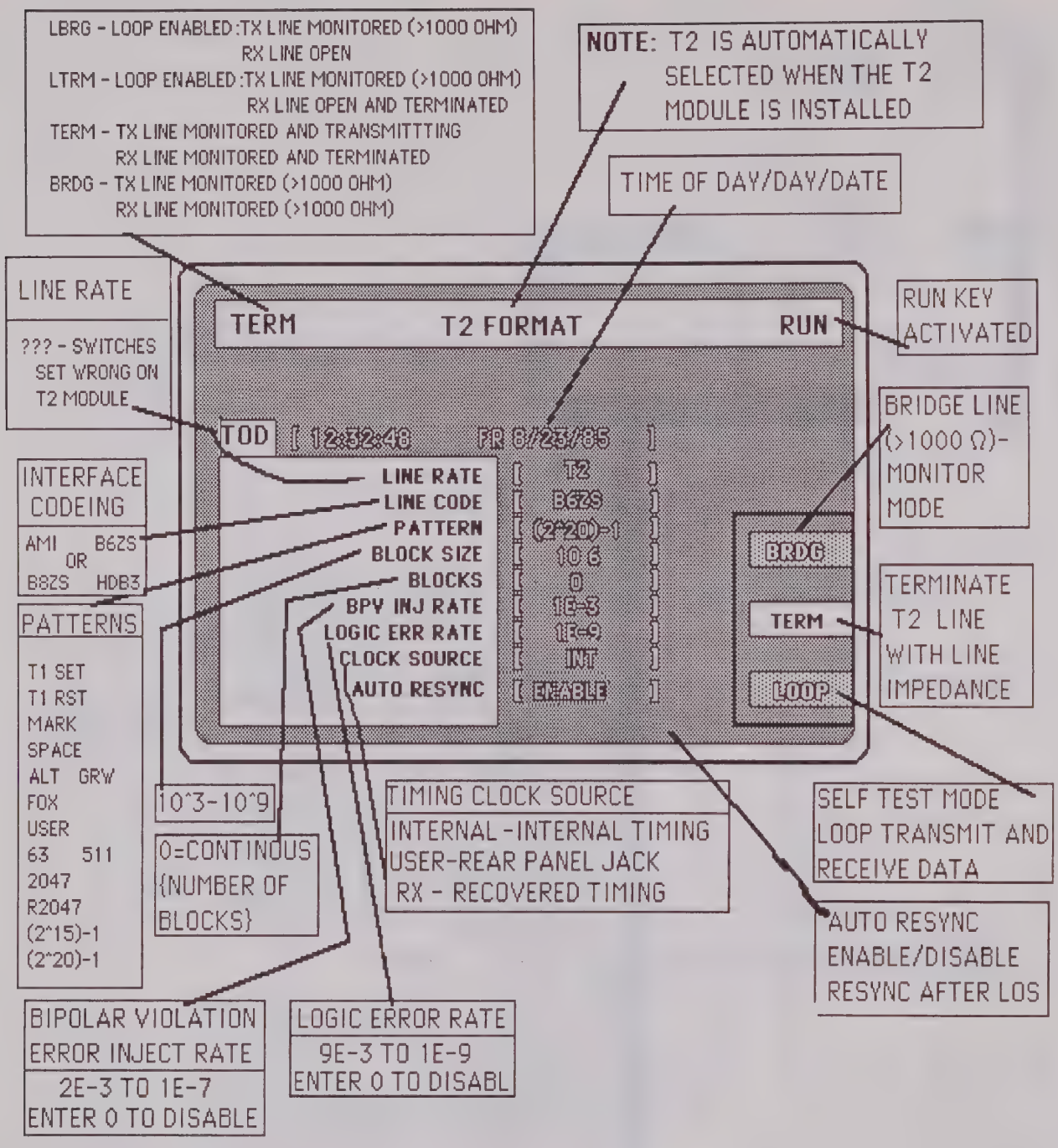


Figure 2-2. T-2 Format Menu

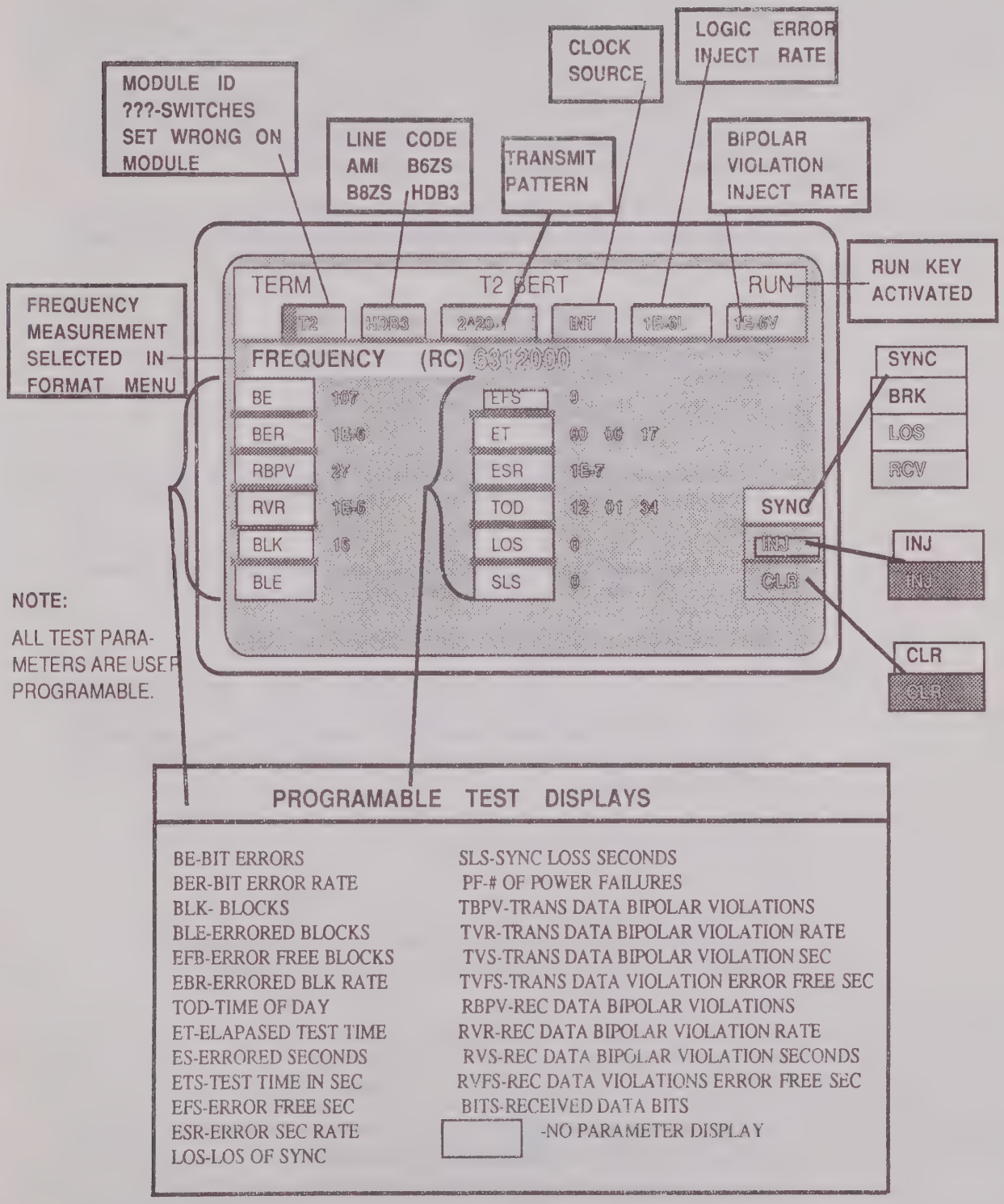


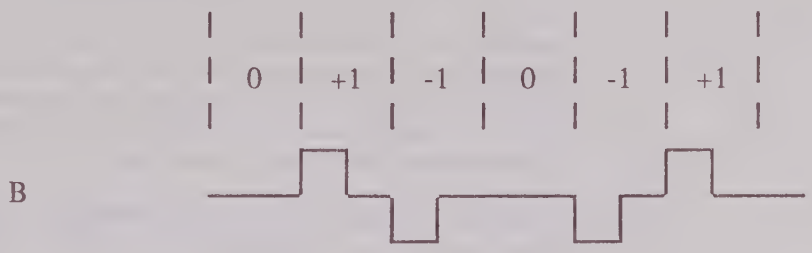
Figure 2-3. T-2 BERT Display

Table 3-1. BERT Format Definitions

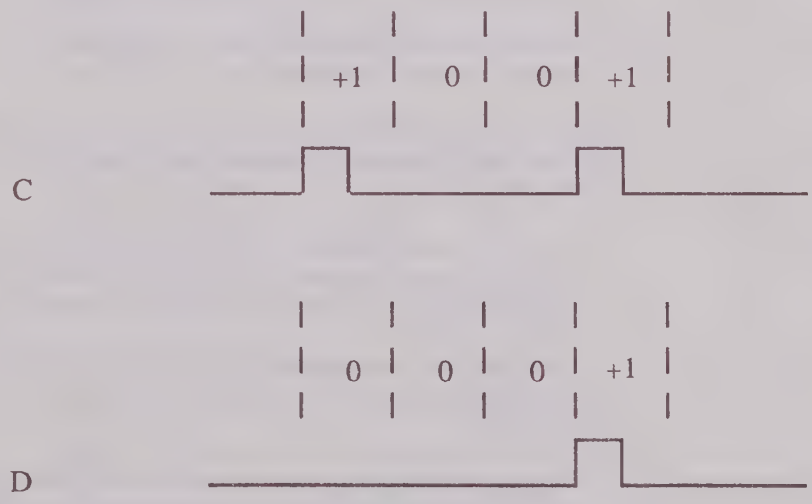
ITEM	DEFINITION
LINE RATE	This block displays the line rate as T1, T1C, or T2 for U.S. systems or 2.048 and 8.448 Mbps for CCITT G.703 modules. This is not a selectable parameter but is fixed by the interface module inserted into the Model 5500. It is a convenience item to remind the operator of the rate at which the Model 5500 is testing.
LINE CODE	The line code of the T-Carrier system under test may be selected by moving the half intensity block over the LINE CODE window and using the SELECT keys to choose the options. The options are: T1 AMI or B8ZS T1C AMI or B8ZS T2 AMI or B6ZS 2.048 Mbps AMI or HDB3 * 8.448 Mbps AMI or HDB3* * 2.048 Mbps and 8.448 Mbps G.703 modules are set for HDB3 at the factory and T-2 modules are set for B6ZS. A DIP switch on the module allows selection of AMI coding. The Alternate Mark Inversion (AMI) or Bipolar line code is the line code currently in use in the U.S. on all T1 baseband source code into AMI line code. Note that successive MARKS (1's) always alternate in polarity. A new format, Bipolar 8 Zero Substitution (B8ZS), is being considered for T1 in order to remove the restrictions on the number of successive SPACES (0's) which AMI places on the source coder. While not in actual use at the present time, this line code may become the future standard. An example of a B8ZS coded signal is provided in figure A. 0 0 0 V 1 0 V 1 Assuming the last 1 transmitted was a positive "one". The polarities of the substituted word are simply reversed if the last "one was negative. 0 0 0 0 0 0 0 0 original word 0 0 0 +1 -1 0 -1 +1 substituted word BPV's always occur at the 4th and 7th bit positions of the substituted word. The line code used by T2 carrier systems is B6ZS which is similar to the B8ZS code previously discussed but which limits strings of 0's to less than 6. In this case a block of six consecutive zeros is substituted by the sequence "0 + - 0 - +" if the preceding mark was positive, or "0 - + 0 + -" if the preceding mark was negative (+ or - represents a positive or negative mark). An example of B6ZS coding is shown in figure B.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION



Finally, High Density, Bipolar 3 Zero Substitution (HDB3) line coding is used in European T-Carrier systems at 2.048 MBPS and 8.448 MBPS line rates. An example of this coding format is shown if figures C and D. (Preceding violation was negative and preceding pulse was negative in figure C and the preceding violation was negative and the preceding pulse was positve in figure D.)



The HDB3 coding process generates positive and negative marks alternately each time a binary logical 1 condition occurs within the message signal. However, unlike AMI coding, the maximum number of consecutive zeros is limited to a value of 3. If a series of 4 consecutive zeros does occur, the 4th zero is replaced by a mark referred to as a VIOLATION. The violation mark is always inserted with the same polarity as the preceding mark. This identifies the departure from the AMI scheme and indicates the occurrence of the violation.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
	In theory, if additional safeguards were not taken, it would be possible for several violations to have an identical polarity, and thus introduce a DC component into the signal. To overcome this problem, the coder continuously monitors the polarity of the last violation (may have been many bits earlier in the data stream) and the polarity of the last mark. The coder then forces the first bit of the 4-bit substitution sequence to a one or a zero, whichever is required, to allow the violation in the fourth bit position to be of opposite polarity to the previous violation.
PATTERN	The pattern choices from the regular FORMAT are all present in T-Carrier FORMAT, but the most useful patterns for T-Carrier testing are:
QRW QUASI-RANDOM WORD	A pattern of (2^20)-1 bits long which has built-in suppression of strings of 0's greater than 14. This pattern is the industry standard for T1 and T1C testing. (2^15)-1: A pseudo-random sequence used in European CCITT G.703 BER testing and jitter testing. (2^20)-1: A pseudo-random sequence of the same length as the QRW, but without the 14 zero suppression. Useful at T2 and for CCITT testing.
MARK	An all 1's pattern which may be used to simulate the "idle" pattern sent out by digital channel banks in an alarm condition.
USER	This is a user definable pattern of up to 135 characters (1080 bits) which could be used to send out patterns with more than 14 zeros or any other pattern a user may want to transmit.
T1 SET	This pattern sends out the standard T1 Channel Service Unit (CSU) loopback code (10000) to cause a remote CSU to loopback for test purposes. This code should be transmitted for 5 seconds before the CSU will loopback to prevent false loopbacks.
T1 RESET	This pattern sends out the standard T1 CSU reset code to return a CSU in loopback to normal operation. The code (100) should be sent out for 5 seconds to reset CSU loopback.
BPV INJ RATE	The user may select any rate of injection of Bipolar Violations from 2^{-3} to $1x^{-7}$ violation/bit. The rate is selected by changing the mantissa from 0 to 9 (a 0 disables the inject function) first and then moving the half intensity block to the right and changing the exponent from -3 to -7 as desired. The select keys or the HEX keypad can be used. A common rate is 1^{-3} which is useful in checking automatic protection switches. Pressing the INJ soft key on the main BERT display activates BPV Injection unless there is a "0" in the BPV in the inject rate mantissa.
LOGIC ERR RATE	Logic errors are what telephone companies call bit errors to distinguish them from BPV's. This rate of bit error injection is selectable from 9x10-3 to 1x10-9 errors/bit. The errors (and bipolar violations) are uniformly spaced throughout the bit stream when the INJ soft key is pressed. Note that the user is free to have either logic errors or BPV's or both injected.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
CLOCK SOURCE	The user may select from three alternatives depending upon what simulation is being attempted. When the Model 5500 is acting as the generator of the T- Carrier it is normal to choose INTERNAL timing so that the Model 5500 is the master clock. This would be the case whenever any loopback testing is performed. The "RX" or Receive Clock choice allows the user to operate a 5500 in what is called a loop timed mode. That is, the Model 5500 derives clock from the received bit stream and uses this to time its transmitter. This is useful if, for example, the user is making an end to end bit error test with Model 5500's at each end. In this case one of the test sets should be on INTERNAL (acting as the master clock) and the other should be set to RX. The final option available is USER which allows the operator to supply a TTL clock to the rear panel BNC connector. The clock supplied must be at the nominal bit rate of the module being used (i.e. 1.544 MHZ for T1 module, 6.312 MHZ for T2, etc..), and should be at least + 30ppm accurate.

Table 3-2. BER Test Assistance

SYMPTOM	POSSIBLE CAUSE
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Verify that BRIDGE mode in T- Carrier testing has not been selected. (BRIDGE mode disables the Model 5500 transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units.
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.
Test suddenly stops and RUN LED goes off	If continuous testing is desired verify that '0' has been placed in the Number of Blocks test window and press RUN. If testing a specific number of blocks verify that the number of blocks selected has been reached when test set stops. This is normal operation.
Model 5500 display errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. NOTE: T1 carrier systems are only specified to provide a 1x10-6 error/bit rate which is about three errors or less every two seconds.

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Model 5500-800

CCITT G.703 2.048 Mbps Interface Module

1.0 INTRODUCTION

Operation of the G.703 2048 KBPS Interface Module for the Model 5500 Analyzer is very similar to that specified for the DS-1/DS1C (T1/T1C) Interface Module.

The G.703 module differs from the T1/TC module only in the receiver/transmitter signal levels, impedance, line coding and Bit Rate. Specifically, the G.703 module operates at 2048 KBPS with HDB3 line coding, 2.37V peak nominal pulse amplitude at 75 ohms (input and output impedance) with co-ax TX and RX connectors. The G.703 module operating modes and test capabilities are otherwise identical to those of T1/T1C modules. This includes Bert testing with measurement and/or injection of Bit Error (BE) and or Bipolar Violations (BPV's) in terminated, bridged, or loop (self test) configurations.

2.0 DESCRIPTION

In the BRDG mode, two independent receiver circuits are active (refer to figure 2-1). The RX receiver provides all BERT, Frequency, BPV etc. measurement parameters in both the BRDG and the TERM modes. A second TX receiver (high impedance) provides BPV and Frequency measurement for whatever line is connected to the TX connector.

NOTE: The BPV measurement provided by the G.703 module when using the HDB3 line code maybe a valid and useful parameter in that only BPV's which do not belong to a valid HDB3 substitution code are counted.

However, due to the nature of the HDB3 line code, the use of the BPV inject function (applicable only in the TERM Mode) will result in a combination of Bit Errors and a BPV rate measurement which does not match the BPV's inject rate. This results because injected BPV's will alter the random BERT data to falsely resemble HDB3 substitution code sequences and cause the receiver circuit to translate those false HDB3 sequences into a string of 4 logic zeros - causing Bit Errors.

Both the TX and RX receivers have Automatic Line Build Out (ALBO) circuits which allow operation of the G.703 module at any point up to several thousand feet from the transmitter - in either the TERM or the BRDG mode.

3.0 OPERATION

The G.703 FORMAT Menu will allow selection of either the HDB3 or the B6ZS line code; however, selection of the B6ZS line code is not applicable to standard G.703 operation (consult factory if B6ZS operation is required).

The G.703 module may be configured to provide a 75-ohm line termination (TERM) or may be operated in a high impedance bridge (BRDG) connection to an otherwise terminated line. The BRDG mode may be used with direct connection to the line or may also be used with isolating resistors of 482 ohms maximum in series with each side of the line (equivalent to a standard American Telephone DSX "Monitor" test point).

NOTE: The BRDG high impedance mode should be used even if 430 ohm series resistors are used in a "Monitor" test point. The LOOP configuration provides a self test mode by connecting the TRANSMITTER output to the RECEIVER input.

NOTE: It is not necessary to disconnect the G.703 module from the line under test when selecting LOOP mode. Relays in the G.703 module disconnect the transmitter and receiver from the external line when LOOP is selected.

TERM, BRDG, and LOOP modes are selected by using the soft keys for the G.703 FORMAT Menu (similar to the T1/T1C FORMAT Menu).

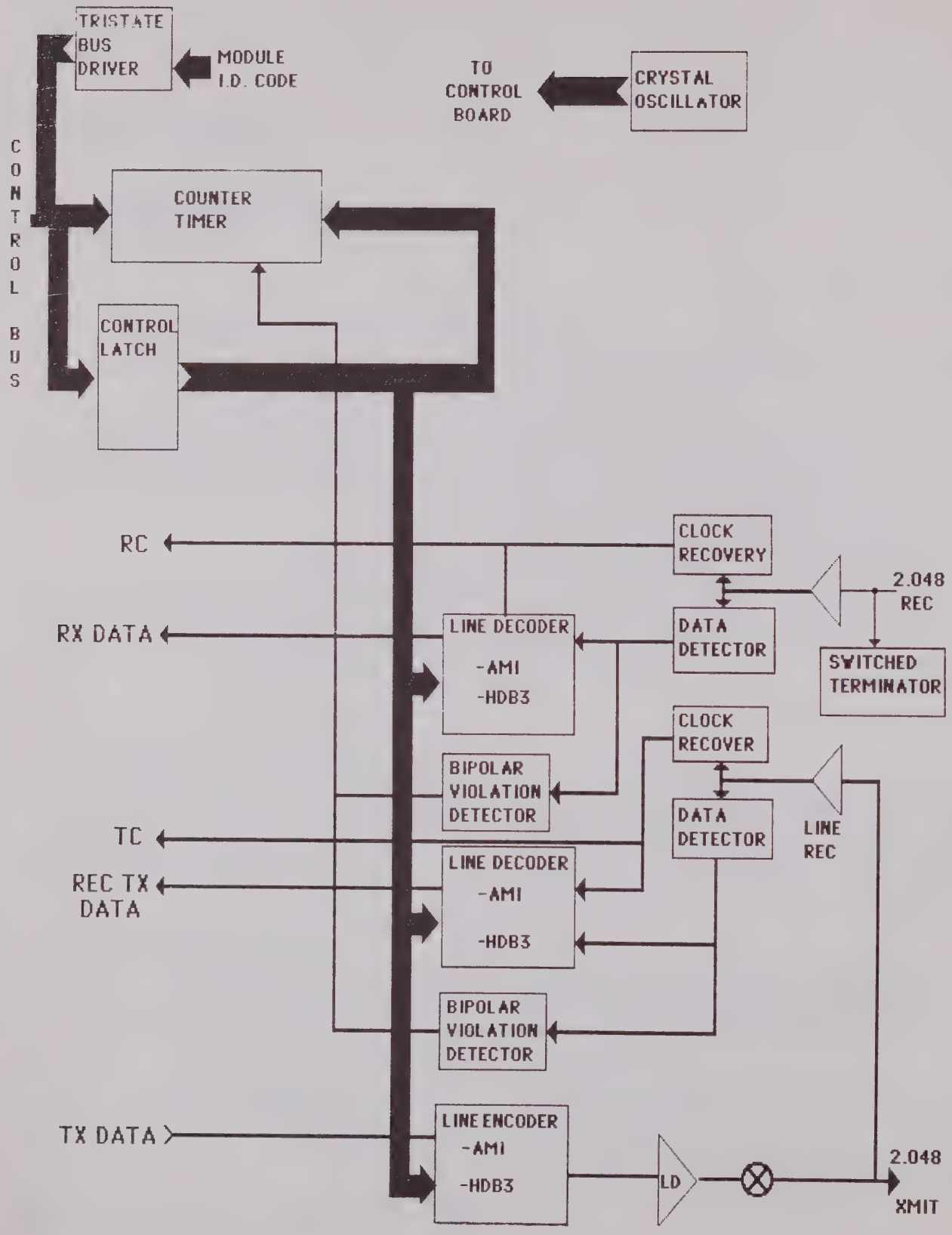

Figure 2-1. Model 5500-800 Interface Module Block Diagram

Model 5500-805

CCITT G.703 8.448 Mbps Interface Module

1.0 INTRODUCTION

The Model 5500-805 G.703 8448 Kbps Interface Module enables the Model 5500 to test data communication systems operating at G.703 8448 Kbps rates in accordance with the CCITT G.703 specification. The module provides the capability to transmit and receive data at the 8448 Kbps rate, in either HDB3 or AMI line code Formats, utilizing bipolar transmission techniques.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-805 Interface Module.

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-805 module enables the Model 5500 to generate and receive G.703 8448 Kbps serial data streams, recover clock, and regenerate data from low level signals. The mechanical interface between the module and the system under test consist of BNC type connectors for transmit and receive data, each with a separate grounding lug that enables the user to terminate the coaxial shield if desired, and a 15 pin subminiature D-type connector for transmit and receive data (used by some modem manufacturers) whose pins are in parallel with the transmit and receive BNC connectors.

The Generator section (refer to figure 2-1) consists of a line encoder, and a line driver. The line encoder can be configured to produce an AMI or HDB3 line code for the bit stream at the 8448 Kbps rate.

Table 2-1. Model 5500-805 Interface Module Specifications

CHARACTERISTIC	SPECIFICATION
TRANSMITTER	
Pulse Rate	8448 Kbps + 30 ppm
Output Pulse Amplitude	+2.37 v peak +10%
Output Pulse Shape	Rectangular
Overshoot	Less than 10% of amplitude height.
Line Code	HDB3 or AMI (User Selectable)
RECEIVER	
Input Impedance	75 ohms + 5% terminated. >1000 ohms bridged.
Input Level	+2.37 v peak plus up to 2000 ft. coaxial cable.

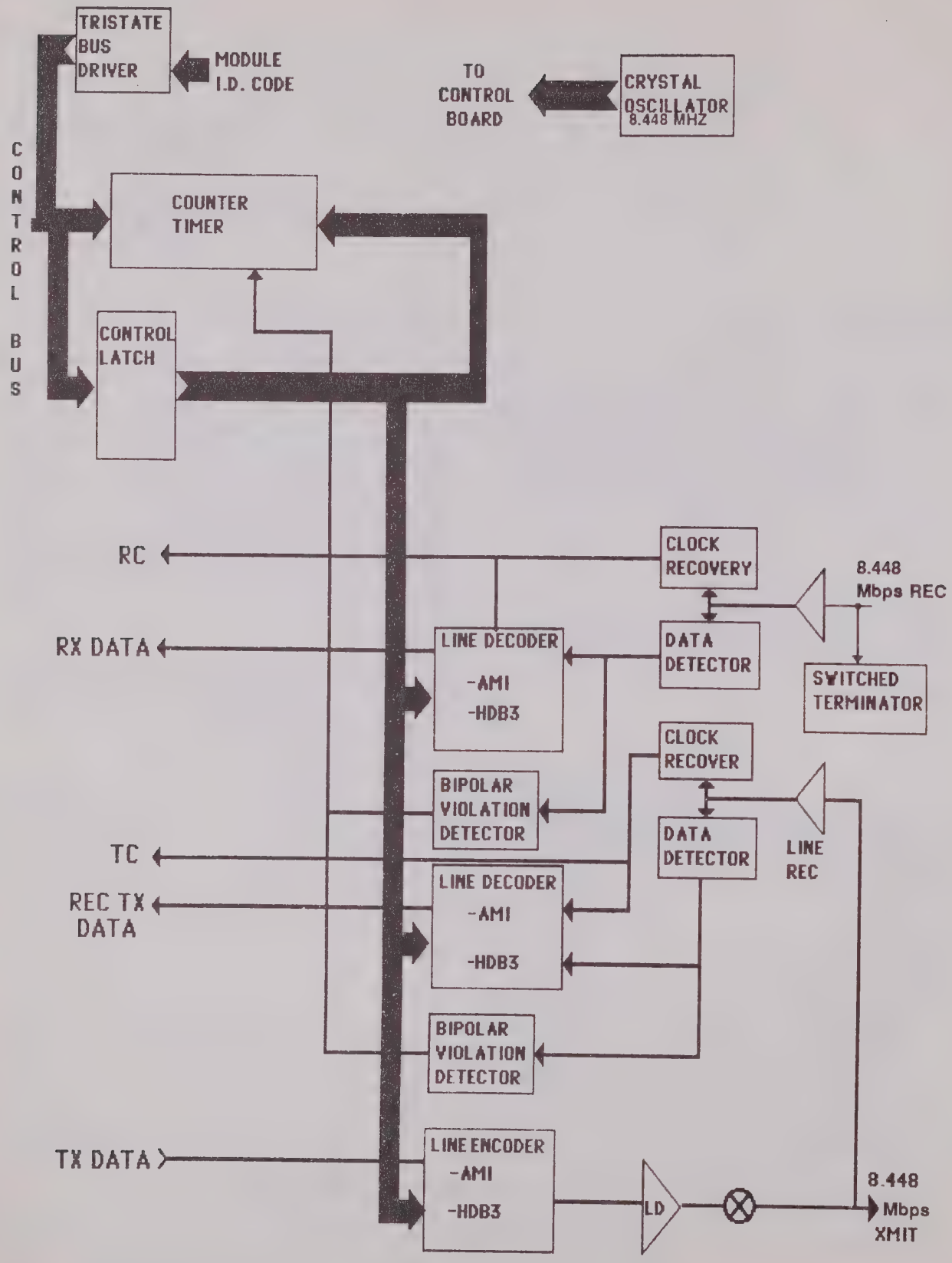

Figure 2-1. Model 5500-805 Interface Module Block Diagram

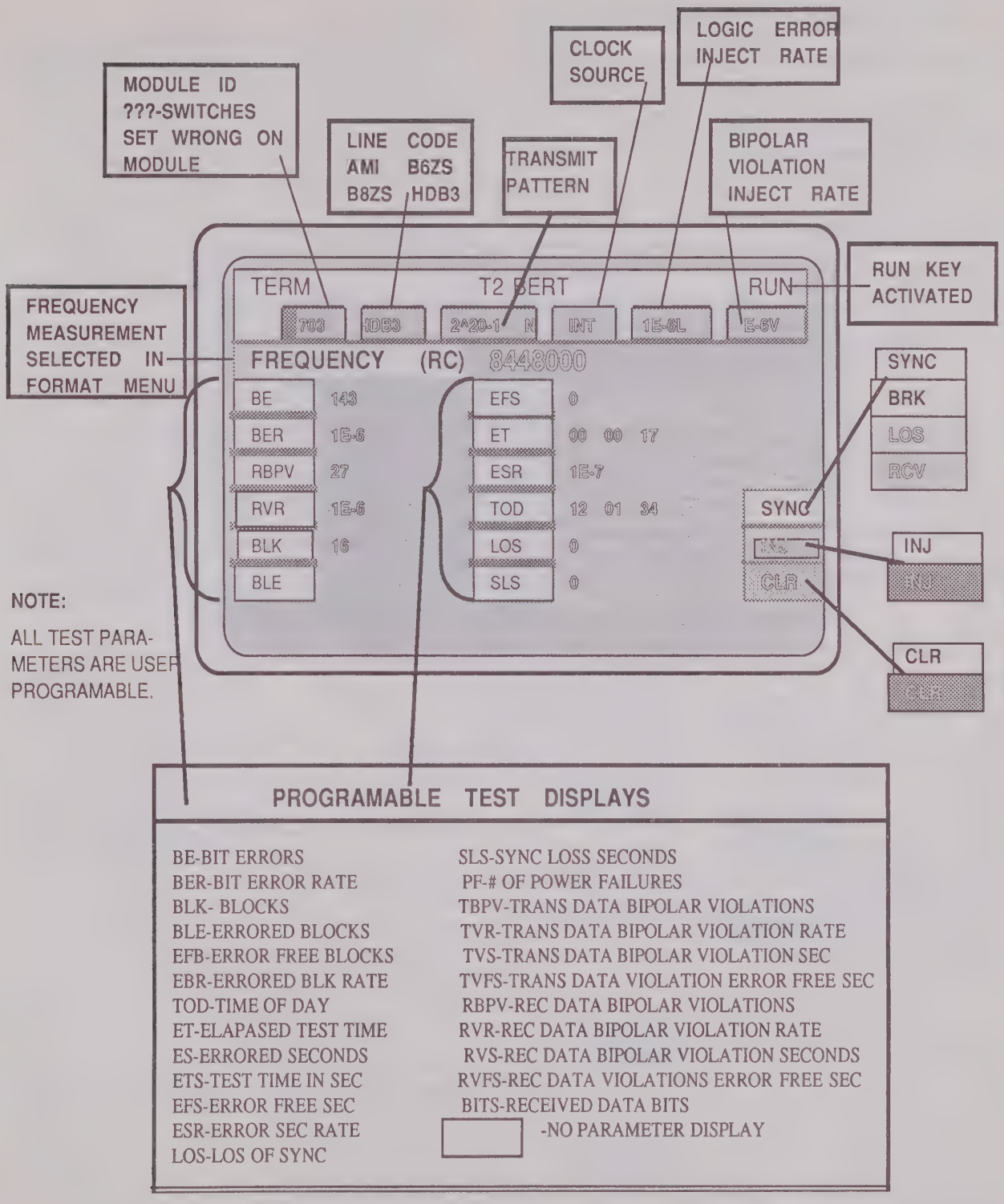

Figure 3-1. Model 5500-805 BERT Display

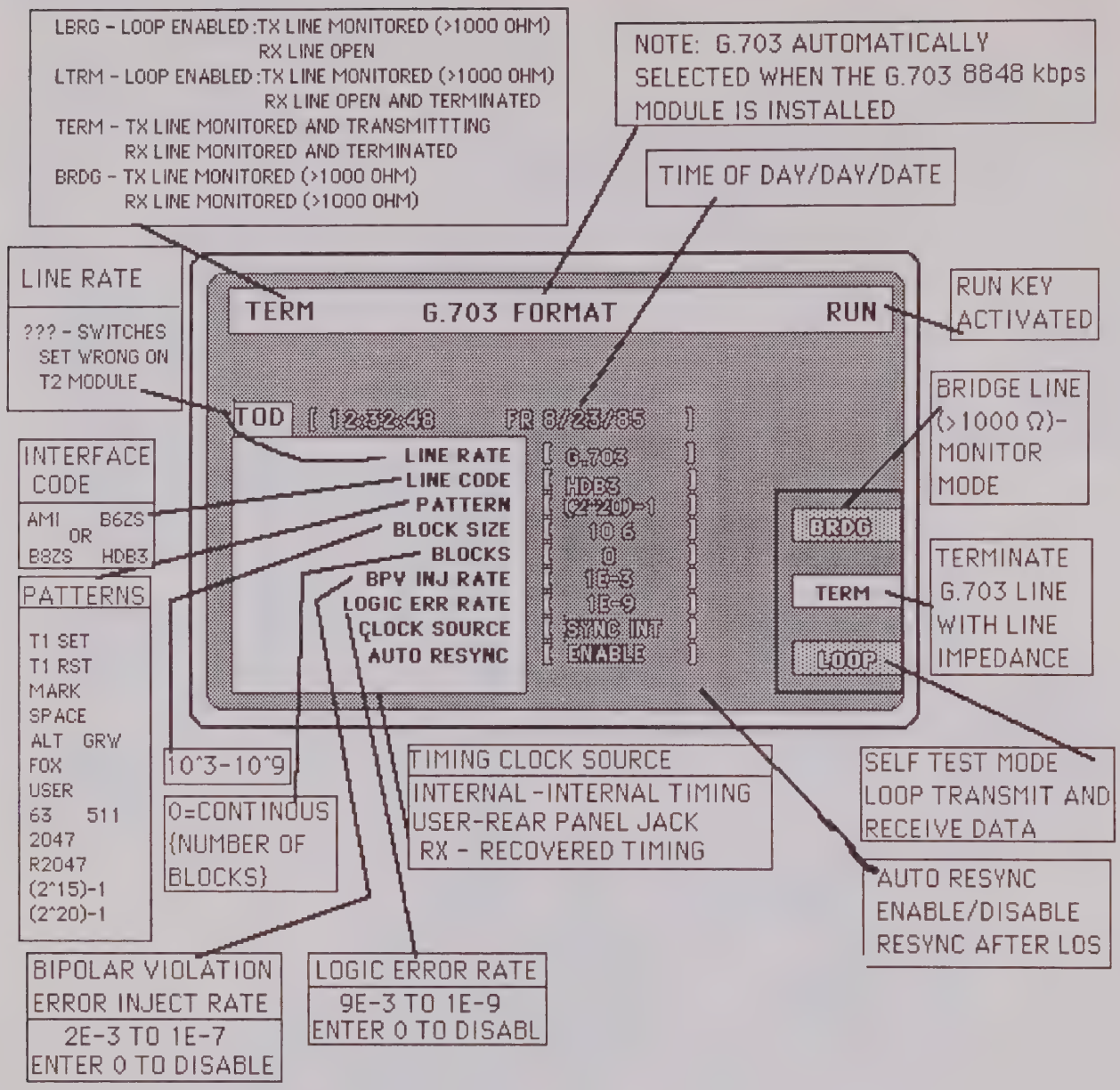

Figure 3-2. Model 5500-805 BERT Format

The receive section of the module contains two independent receivers. This configuration enables the Model 5500 to monitor both receive pair and Transmit pair traffic for Bipolar Violations. The Receive input has a switchable line termination to enable it to receive input signals and terminate them in 75 ohms, as well as monitor signals in a Bridged mode. With the exception of the switchable impedance each receiver is the same. The receiver section recovers and regenerates the signal at the cross connect point. The clock recovery circuit (basically a phase locked loop) derives timing from the incoming bit stream and feeds it to the data detector, line decoder, and Model 5500 internal logic. The Receive Clock and received Transmit Clock are both recovered in this manner.

The Data Detector accepts the output signal of the Receiver and combines it with the recovered clock to do the final reshaping and regeneration of the input which is then passed to the Line Decoder and Bipolar Violation Detector. The Line Decoder is set to AMI or as appropriate and converts the line coded signal to a TTL level bit stream for analysis by the Model 5500 internal logic. The BPV detector compares the output of the Data Detector to the AMI coding rule and passes information on violations of the rule to both the line Decoder and Counter Timer circuits which in turn initiate the count of BPV's displayed on the CRT.

3.0 OPERATION

The Model 5500 G.703 BERT Display and Format Menus (refer to figures 3-1 and 3-2) contain an area that displays the line code. When position 1, SW3, of the G.703 8448 Kbps Interface Module is in the "ON" position, these display areas will display "B6ZS" or "HDB3". When the switch is in the "OFF" position, these display areas will display "AMI" or "B8ZS". Since G.703 8448 Kbps will only utilize AMI or HDB3, the proper line code may be selected via the menu soft keys once the switch on the G.703 8448 Kbps Interface module has been placed in the desired position.

In the HDB3 mode of operation the Line Decoder and Bipolar Violation Detector combine to ignore intentional Bipolar Violations.

3.1 LINE MODE SELECTION

Selection of the desired line mode is performed in the following manner:

1) Remove the top cover of the G.703 8448 Kbps Interface Module, held in place with four Phillips head screws.

2) Carefully separate the top PC board (G.703 8448 Kbps I/O Module Board) from the bottom PC board (G.703 8448 Kbps Control Board) and remove the transmit and receive cable connectors from the top PC board.

3) Configure SW3, position 1, for the desired line code (refer to figure 3-3). Select "ON" for HDB3 or "OFF" for AMI.

4) Reassemble the module, taking care not to bend any of the pins on the connectors between the top and bottom PC boards.

NOTE: Positions of switches other than SW 3, position 1, are shown for illustration **ONLY**, and may or may not reflect the switch positions set at the factory for your card.

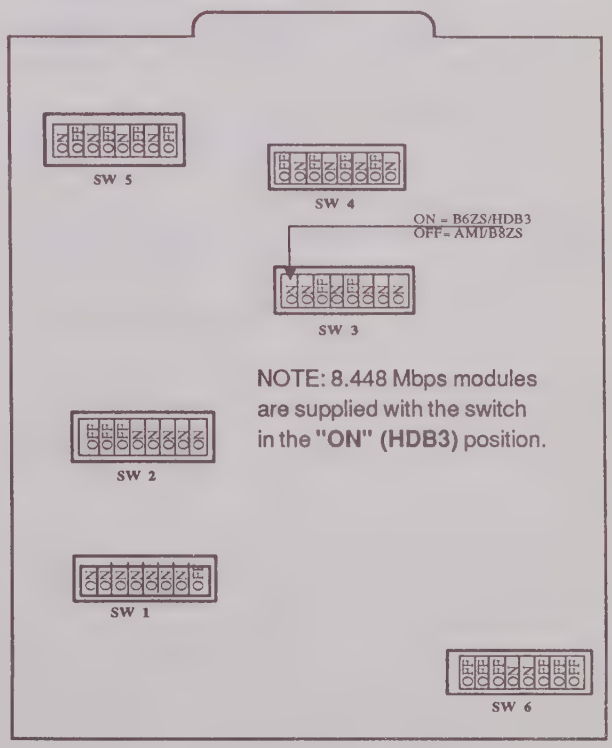

Figure 3-3. G.703 8448 Kbps Line Code Selection

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Model 5500-J01

Low Speed Jitter Option

1.0 INTRODUCTION

The Model 5500-J01 option enables the user to measure low speed (75 to 72000 bps) jitter and read the results on the main BERT display. The J01 option consists of a printed circuit card which is mounted in the bottom of the 5500 chassis. Control, status, and data interface signals are connected to the 5500 control board via a 34 pin ribbon cable. Power, consisting of +5 VDC and ground, is received thru the board on a 2 pin connector cabled to the main power supply.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-J01 low speed jitter option.

2.1 FUNTIONAL DESCRIPTION

The 5500-J01 option uses a sampling technique to measure edge timing difference on the received data. The received data is sampled at approximately 250 times the bit rate. The result of this sample is used to synchronize an internal clock to the average data transitions.

Edge jitter is then calculated by measuring the percent of difference between the actual transitions of the received data and the transitions of the synchronized internal clock.

It should be noted that this sampling technique depends on transitions to acheive accuracy and synchronize the internal clock. Therefore, long periods of one's (1's) or zero's (0's) may result in inaccurate readings.

3.0 OPERATION

The 5500-J01 option permits the display of measured jitter results as four different readings (all as a percent of bit period) on the main BERT display (refer to figure 3-1). These readings will continually vary if the FRE mode has been selected or will be presented as a peak hold reading in the HLD mode. When the HLD mode is selected, the reading displayed will be the largest reading obtained after depressing the CLR switch to begin the test.

The four readings are:

pp Represents peak-to-peak or the largest differences in edges during 1024 samples at frequencies above 300 bps or 256 samples below 300 bps.

+p Represents the largest difference in data edges that is later than the internal oscillator.

-p Represents the largest difference in data edges that is earlier than the internal oscillator.

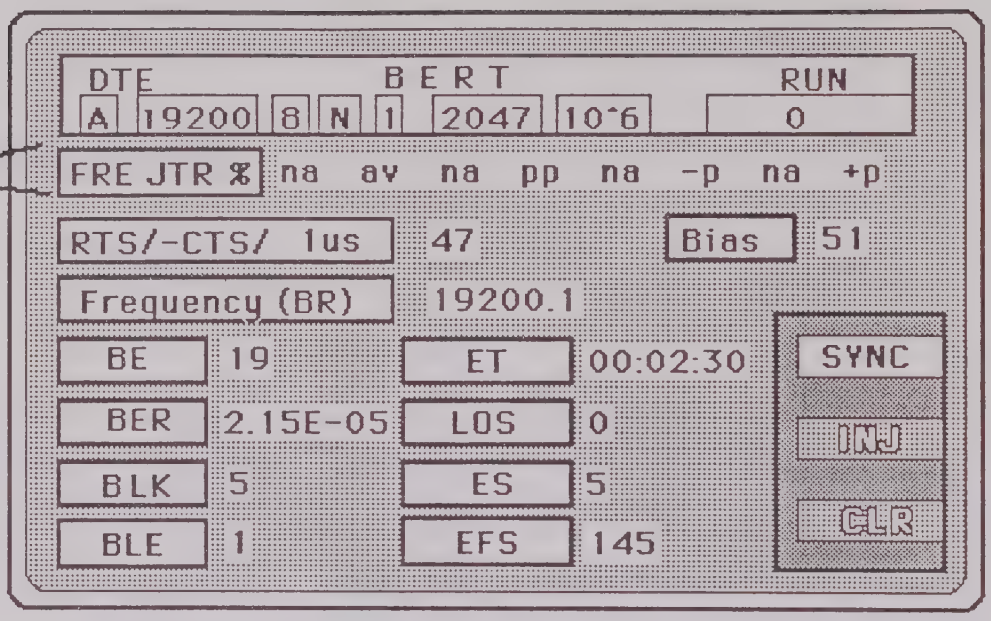
av Represents the average difference between data edges, sampled over the same 1024 or 256 bit period as the **pp**, **+p**, and **-p** readings.

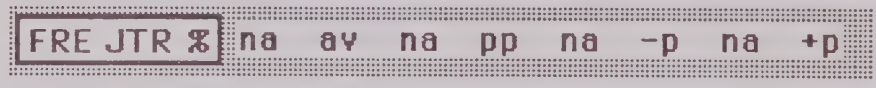
4.0 MAINTENANCE

Since the 5500-J01 option uses an all digital approach, no setup or adjustment is required. An occassional frequency check may be desirable, to insure the calibration of the 18.432 MHz oscillator.

Table 2-1. Model 5500-J01 Specifications

CHARACTERISTIC	SPECIFICATION
FREQUENCY RANGE	75 bps to 72000 bps at standard bit rates.
ACCURACY	± 1.0 %
OFFSET	± 1.0% maximum except for 134.5 and 56000 Hz ± 2.0% at 134.5 and 56000 Hz





This line from the main BERT display is used with the J01 Option.

FRE	Displayed when the free run mode is selected.*
HLD	Displayed when the hold mode is selected.*
na av	na appears when J01 option is not installed and/or not in use.
0 av	numeric value (0-99) of readings when J01 option is in use.

* only operator selections available in jitter measurement.

NOTE: For information on all aspects of this display, refer to figure 3-4 in the Operation section of this instruction book.

Figure 3-1. Model 5500-J01 BERT Format

Model 5500-300

CCITT V.35 Interface Module

1.0 INTRODUCTION

The Model 5500-300 CCITT V.35 Interface Module option is designed to permit the Model 5500 to be configured to test both DCE and DTE devices. This CCITT Recommendation (V.35) covers data exchanged in a serial format with a synchronous clock in a balanced mode. The cable lengths usable with the V.35 interface decreases sharply as the data rate increases and while it may be possible to operate at rates up to 7 Mbps, the cable between test set and device should be kept as short as possible at these rates.

2.0 DESCRIPTION

Table 2-1 presents the Model 5500-300 CCITT V.35 Interface Module specifications. Table 2-2 presents the connector pin assignments.

2.1 FUNCTIONAL DESCRIPTION

A block diagram of the V.35 interface module is presented in figure 2-1. The DCE and DTE I/O connectors provide the mechanical interface between the Model 5500 and the equipment under test. The DCE is male and DTE is a female connector.

Table 2-1. Model 5500-300 Specifications

CHARACTERISTIC	SPECIFICATION
Mode	Synchronous
Emulation	DCE or DTE
Data Rate	7 MHZ maximum (dependent upon cable length).
Balanced Drivers	Terminal-to-Terminal
Voltage Swing	±.55 Volts ± 20% into a 100 ohm resistive load.
	Source Impedance: 100 ±10% ohms
	Rise Time: Less than 40 nsec
Balanced Receivers	Load Impedance: 100 ±10% ohms
	Resistance between shorted terminals to ground: 150 ± 10%ohms.
Unbalanced Drivers (RS-232 C/V.28)	Output Voltage: ±9.0 ±2.0 v. peak
	Output Impedance: 300ohms minimum
	Slew Rate: 30.0 volts per microsecond maximum.
	Short Circuit Current: 12maximum.

Table 2-1. Model 5500-300 Specifications (Cont)

CHARACTERISTIC	SPECIFICATION
Unbalanced Receivers (RS-232C/V.28)	MARK Voltage: -5.0 volts maximum SPACE Voltage: +5.0 volts minimum Maximum Input Voltage: ±25 Volts Load Impedance: 3000 to 7000 ohms MARK Voltage: 0.0 volts maximum SPACE Voltage: 2.0 volts minimum

Table 2-2. Connector Pin Assignments

PIN	CIRCUIT	DESCRIPTION
A	AA	PROTECTIVE GROUND
B	AB	SIGNAL GROUND
C	CA	REQUEST TO SENT
D	CB	CLEAR TO SEND
E	CC	DATA SET READY
F	CF	RECEIVED LINE SIGNAL DETECTOR
H	CD	DATA TERMINAL READY
J	CE	RING INDICATOR
K	-	LOCAL TEST
L		UNASSIGNED
M		UNASSIGNED
N		UNASSIGNED
P	SD (A)	SEND DATA
R	RD (A)	RECEIVED DATA
S	SD (B)	SEND DATA
T	RD (B)	RECEIVED DATA
U	SCTE (A)	SERIAL CLOCK TRANSMIT EXTERNAL
V	SCR (A)	SERIAL CLOCK RECEIVE
W	SCTE (B)	SERIAL CLOCK TRANSMIT EXTERNAL
X	SCR (B)	SERIAL CLOCK RECEIVE
Y	SCT (A)	SERIAL CLOCK TRANSMIT
Z		
AA	SCT (B)	SERIAL CLOCK TRANSMIT
BB		
CC		SPARE
DD		UNASSIGNED
EE		SPARE SIGNAL

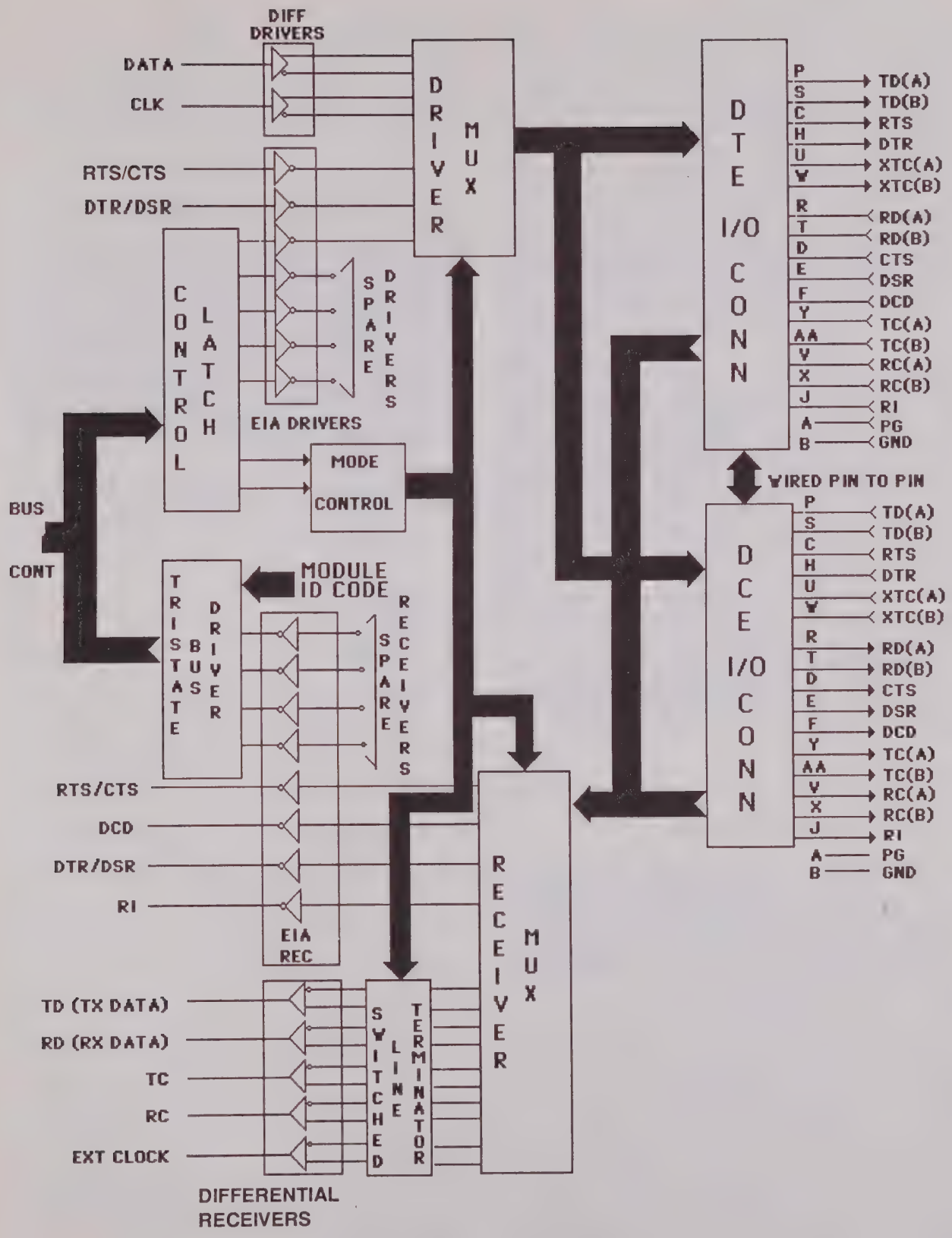


Figure 2-1. Model 5500-300 CCITT V.35 Interface Module Block Diagram

The electrical interface between V.35 equipment and the internal TTL levels is accomplished by the balanced differential drivers and receivers. The signaling information such as RTS, CTS and other DC signals is converted using the EIA RS-232 drivers and receivers in accordance with CCITT recommendation V.28. The Receiver Multiplexer takes signals from DCE and DTE connectors, and feeds them to the appropriate balanced differential, or EIA receiver for conversion to TTL level and processing within the Model 5500 logic. The Receiver Multiplexer also feeds the appropriate received data and clock signals through the switched line terminations before the balanced receivers. The Mode Control logic controls the configuration of the Module for DCE or DTE testing, and selects the appropriate terminating impedance as well as the operation of the Receiver and Driver Multiplexers to generate and receive the correct signals on the DCE or DTE I/O connectors. The Model 5500 logic controls the operation of the interface module through the control bus which interfaces to the module through the TRI-STATE BUS Driver and Control Latch devices. The Module ID code, which informs the Model 5500 that the V.35 module is plugged in, feeds into the Tri-State Bus Driver along with spare EIA receivers for future enhancements. The Control Latch converts the information on the Control Bus to signals to drive the Mode Control logic to simulate DCE or DTE Modes of operation. The balanced differential drivers and EIA drivers are fed to the appropriate pins on the DTE and DCE I/O connectors by the Driver Multiplexer which is controlled by the Mode Control logic.

3.0 OPERATION

3.1 DTE CONFIGURATION

The DTE Mode is selected by toggling the DCE/DTE front panel key to obtain the DTE indication on the CRT display. In the EXTERNAL CLOCK mode, the Model 5500 derives its timing from the DCE under test on the Serial Transmit Clock leads Y and AA or from the USER CLOCK BNC connector.

In turn, the Model 5500 generates Transmit Data and External Transmit Clock on pins P, S, and U, W, respectively. The Model 5500 detects Receive Data on pins R, T, and receive Clock on pins V and X. If the user selects an internal bit rate the Model 5500 becomes the clock source for the test set up. The unit generates transmit data, and clock on pins R, S and U, W, respectively. The internal bit rate of the Model 5500 may be set to any value between 50 bps, and 13 Mbps using the USER CLOCK rear panel BNC jack input to apply an external clock source.

3.1.1 Controls and Indicators

RTS and DTR states are controlled by the front panel keys. DSR, DCD, CTS, RD, TD, RC, TC, and XTC states are also displayed on the front panel LED's.

3.2 DCE CONFIGURATION

When configured as a DCE the Model 5500 generates and supplies clock to the DTE on pins BB and Z (Serial Clock Transmit). The DTE returns Send Data on pins P and S to the Model 5500 in sync with the Serial Clock Transmit on pins BB and Z. The Model 5500 also generates Serial Clock Receive (SCR), and Receive Data (RD) on pins V, X and R, I, respectively and transmits them to the DTE under test. DCD and DSR can be toggled from the front panel keys and all primary leads status indicated on the LED's.

Model 5500-400

RS-449 Interface Module

1.0 INTRODUCTION

The Model 5500-400 RS-449 Interface Module option is designed to provide both the balanced (RS-422) and unbalanced (RS-423) electrical interfaces of RS-449. EIA RS-449 defines two categories of interchange circuits; Category I and Category II. Category I circuits with data rates of 20 Kbps or less may use either the balanced or unbalanced electrical characteristics. Above 20 Kbps all Category I circuits must use the RS-422 balanced characteristics. Category II circuits can use the unbalanced RS-423 electrical characteristics. Examples of Category II circuits are: Select frequency (SF), Signaling Rate Selector (SR), and Signaling Rate Indicator (SI).

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-400 RS-449 Interface Module.

Table 2-1. Model 5500-400 Specifications

CHARACTERISTIC	SPECIFICATION
Mode	Synchronous
Data Rates	DC to 20 Kbps (RS-423) DC to 2.0 Mbps (RS-422)
RS-422 Drivers	Impedance: <100 ohms
	Differential Output Voltage between 2 Volts and 6 Volts.
	Short Circuit Current: less than 150 ma.
	Output Rise Time: less than 20 nsec
RS-422 Receivers	Impedance: 100 ohms
	Differential Input Voltage Threshold: > ± .2 Volts
RS-423 Drivers	Open Circuit Voltage Magnitude between 4 and 6 volts.
	Source Impedance: 50 ohms nominal.
	Output Voltage Magnitude: 3.6 to 5.4 volts with 450 ohm load.
	Short Circuit Current: < 150 ma.
RS-423 Receivers:	Impedance: > 400 ohms
	Differential Input Voltage: > +/- .2 Volts.
Data Mark (Binary 1 or OFF State)	A terminal more negative than B - RS-422
	A terminal Negative Polarity - RS-423
Data Space (Binary 0	A terminal more positive than B - RS-422
	A terminal Positive Polarity RS-423

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-400 EIA-449 interface module option is designed to permit the Model 5500 to be configured as a DCE or DTE device and to test both RS-422 and RS-423 electrical characteristics. The RS-449 standard covers the exchange of synchronous, serial format data in both balanced (RS-422) and unbalanced (RS-423) modes at data rates up to 2.0 Mbps.

A block diagram of the RS-449 Interface Module is presented in figure 2-1. The mechanical interface is provided by two 37 pin I/O connectors; DTE female and DCE male. Table 2-2 presents the RS-449 connector pin assignments.

Signals into the Model 5500 are fed from the DTE and DCE connector pins to the Receiver Multiplexer. The Multiplexer in turn sends the individual signals through the Balanced (RS-422) /Unbalanced (RS-423) jumper strap options for the appropriate selection and then to the switched line terminations for impedance selection. The signals are then fed to the RS-449 Receiver Section for conversion to TTL levels and analysis by the Model 5500. The operation of the module is controlled over the Control Bus which interfaces the Model 5500 to the Control Latch and Bus Driver circuits on the Module. The mode control logic on the interface Module in turn controls operation of the Receiver and Driver Multiplexers and the configuration of the unit as DCE or DTE. Signals to be output from the Model 5500 are fed into the RS-422 or RS-423 drivers as appropriate and the strap options control which type goes to the Driver Multiplexer. The Driver Multiplexer then feeds the signals to their corresponding pins on the DCE and DTE I/O connectors. Certain signals which are always RS-423 are fed directly to RS-423 drivers from the control latch circuitry and then to the I/O connectors.

3.0 OPERATION

The user selects either balanced or unbalanced operation of the RS-449 interface module by changing the jumper straps (refer to figure 3-1) on the interface module. In this manner the individual Category I circuits can be set for RS-422 or RS-423 operation.

Table 2-2. RS-449 Connector Pin Assignments

FIRST SEGMENT ASSIGNMENT			SECOND SEGMENT ASSIGNMENT			CIRCUIT CATEGORY	DIRECTION	
CONTACT NUMBER	CIRCUIT	INTERCHANGE POINTS*	CONTACT NUMBER	CIRCUIT	INTERCHANGE POINTS*		TO DCE	FROM DCE
1	SHIELD	--						
2	SI	A-A'	20	RC	C-B'	II		X
3	SPARE		21	SPARE				
4	SD	A-A'	22	SD	B/C-B'	I	X	
5	ST	A-A'	23	ST	B/C-B'	I		X
6	RD	A-A'	24	RD	B/C-B'	I		X
7	RS	A-A'	25	RS	B/C-B'	I	X	
8	RT	A-A'	26	RT	B/C-B'	I		X
9	CS	A-A'	27	CS	B/C-B'	I		X
10	LL	A-A'	28	IS	A-A'	II	X	
11	DM	A-A'	29	DM	B/C-B'	I		X
12	TR	A-A'	30	TR	B/C-B'	I	X	
13	RR	A-A'	31	RR	B/C-B'	I		X
14	RL	A-A'	32	SS	A-A'	II	X	
15	IC	A-A'	33	SQ	A-A'	II		X
16	SF/SR+	A-A'	34	NS	A-A'	II	X	
17	TT	A-A'	35	TT	B/C-B'	I	X	
18	TM	A-A'	36	SB	A-A'	II		X
19	SG	C-C'	37	SC	C-B'	I	X	

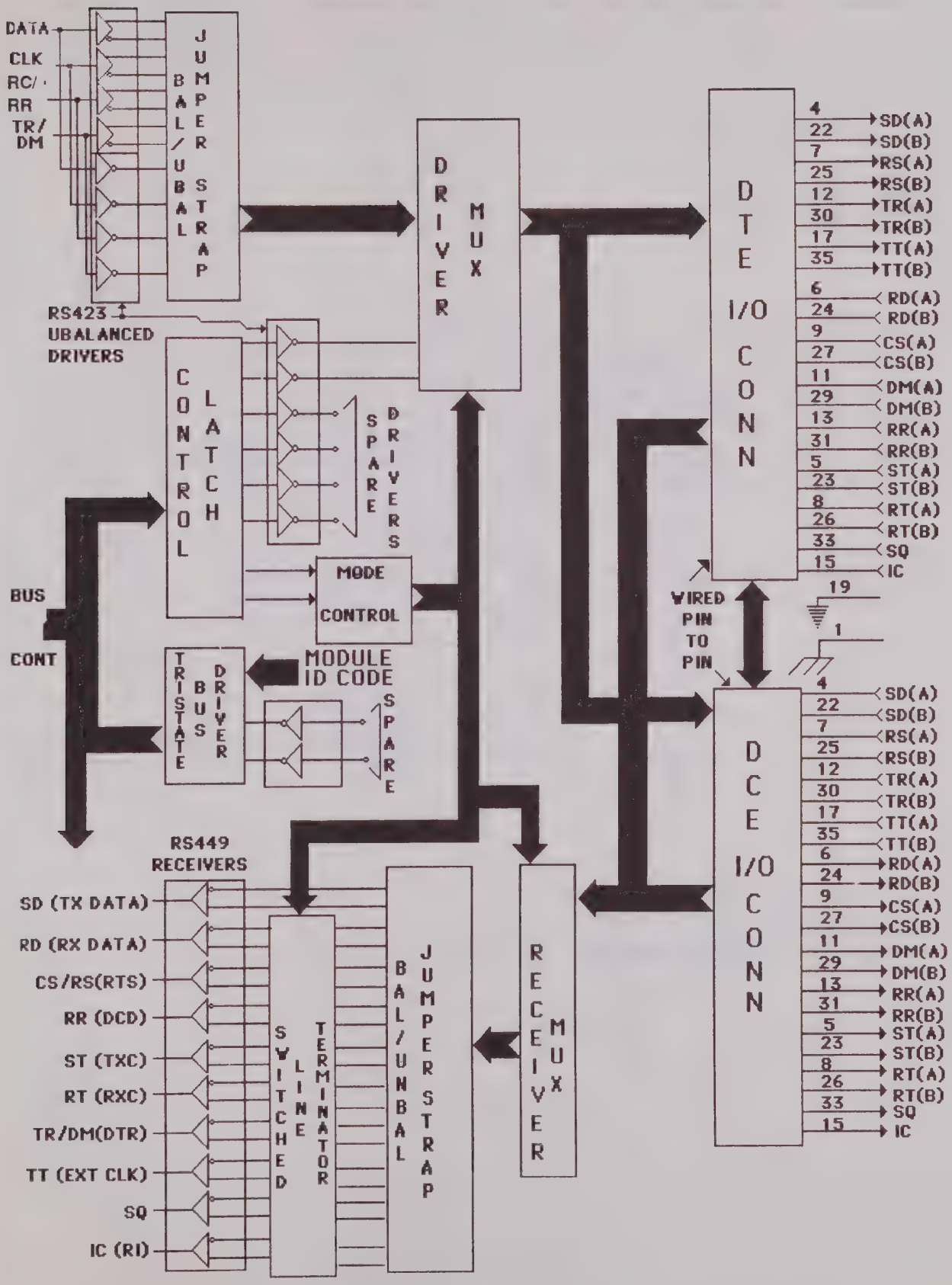
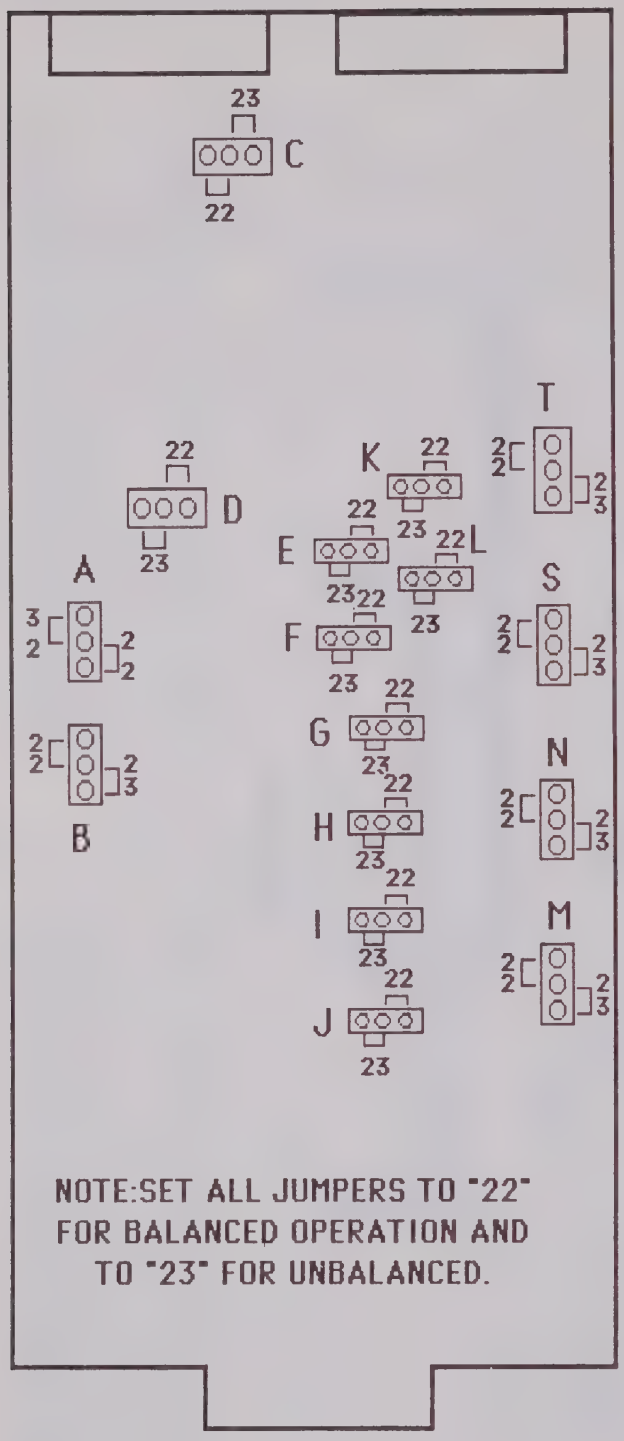


Figure 2-1. Model 5500-400 Interface Module Block Diagram



RS422/423 JUMPERS		RS-449 FUNCTION	
		SIMULATE DTE	SIMULATE DCE
RECEIVER	A	ST	ST
	B	SD	SD
	C	TT	TT
	D	RT	RT
	E	DM	TR
	F	RD	SD
	K	RR	RR
	L	CS	RS
DRIVERS	M	SD(A)	RD(A)
	I	SD(B)	RD(B)
	N	RS(A)	CS(A)
	J	RS(B)	CS(B
	S	TR(A)	DM(A)
	H	TR(B)	DM(B)
	T	TT(A)	ST(A)&RT(A)
	G	TT(B)	ST(B)&RT(B)

NOTE: INDIVIDUAL RS449 SIGNALS MAY BE SET TO 422 OR 423 AS LABELED IN TABLE

Figure 3-1. Jumper Strap Location

Model 5500-450

RS-449/MIL-188-114 Interface Module

1.0 INTRODUCTION

The Model 5500-450 RS-449/MIL-188-114 Interface Module option is designed to provide the balanced (RS-422) and unbalanced (RS-423) electrical interfaces of RS-449 and MIL-188-114. The electrical interface parameters of MIL- STD-188-114 are intentionally and directly equivalent to RS-449 parameters with the exception of the balanced generator offset voltage which is restricted to a value of ±0.4 volts max for MIL-STD-188-114 (RS-449 allows ±3.0 volts max). The model 5500-450 Interface module balanced generators are balanced to ground with offset voltage less than ±0.4 volt; therefore, this module is completely compatible with both MIL-STD-188-114 and RS- 449. EIA RS-449 defines two categories of interchange circuits; Category I and II. Category I circuits with data rates of 20 Kbps or less may use either the balanced or unbalanced electrical characteristics. Above 20 Kbps all Category I circuits should use the RS-422 balanced characteristics. Category II circuits can use the unbalanced RS-423 electrical characteristics. Examples of Category II circuits are: Select frequency (SF), Signaling Rate Selector (SR), and Signaling Rate Indicator (SI).

2.0 DESCRIPTION

Table 2-1 presents the Model 5500-450 Interface Module specifications.

Table 2-1. Model 5500-450 Specifications

CHARACTERISTIC	SPECIFICATION
Mode	Synchronous
Emulation	DCE or DTE
Data Rates	DC to 20 Kbps (RS-423 Unbalanced) DC to 13.0 Mbps (RS-422 Balanced)
RS-422 Drivers	Impedance: <100 ohms Differential Output Voltage between 2 Volts and 6 Volts
	Short Circuit Current: less than 150 ma.
	Output rise Time less than 20 nsec.
RS-422 Receivers	Impedance: 100 ohms terminated >1K ohms un-terminated.
	Differential Input Voltage
	Threshold: > ±0.2 volts

Table 2-1. Model 5500-450 Specifications (Cont)

CHARACTERISTIC	SPECIFICATION
RS-423 Drivers	Open Circuit Voltage Magnitude between 4 and 6 volts.
	Source Impedance: 50 ohms nominal.
	Output Voltage Magnitude: 3.6 to 5.4 volts with 450 ohm load.
	Short Circuit Current: < 150 ma.
RS-423 Receivers	Impedance: 450 ohms terminated. >1K ohms unterminated
	Differential Input Voltage: > ±0.2 volts
Data Mark (Binary 1 or or OFF State)	A terminal more negative than B - RS-422 (Balanced)
	A terminal Negative Polarity RS-423 (Unbalanced)
Data Space (Binary 0 or On State):	A terminal more positive than B - RS-422 (Balanced)
	A terminal Positive Polarity RS-423 (Unbalanced)

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-450 RS-449/MIL-188-114 interface module option is designed to permit the Model 5500 to be configured as a DCE or DTE device and to test both RS-422 and RS-423 (and equivalent MIL-188-114) electrical characteristics. The RS-449/MIL-188-114 standards cover the exchange of synchronous, serial format data in both balanced (RS-422) and unbalanced (RS-423) modes at data rates up to 2.0 Mbps. (The 5500-450 will operate at data rates up to 13.0 Mbps.)

A block diagram of the RS-449/MIL-188-114 Interface Module is shown in figure 2-1. The mechanical interface is provided by two 37 pin I/O connectors; DTE female and DCE male. Table 2-2 presents the RS-449 connector pin assignments.

Signals into the Model 5500 are fed from the DTE and DCE connector pins to the Line Terminator Switch and differential receivers for conversion to TTL levels and analysis by the Model 5500. The operation of the module is controlled over the Control Bus which interfaces the Model 5500 to the Control Latch and Bus Driver circuits on the Module. The mode control logic on the interface Module enables the appropriate tri-state Receivers and Drivers to set the configuration of the units as DCE or DTE.

3.3 OPERATION

Selection of Balanced (RS-422) or Unbalanced (RS-423) drivers is accomplished by activating an alternate action push button switch on the module rear connector panel. Likewise, selection of Terminated or Unterminated receivers is also made with a push button switch. Four LED's indicate the selected mode of operation. When operating in the Terminated mode, the Balanced/Unbalanced switch automatically selects the appropriate termination resistance for each receiver (100 ohms for balanced, 450 ohms for unbalanced).

Table 2-2. RS-449 Interface Connector Pin Assignments

FIRST SEGMENT ASSIGNMENT			SECOND SEGMENT ASSIGNMENT			CIRCUIT CATEGORY	DIRECTION	
CONTACT NUMBER	CIRCUIT	INTERCHANGE POINTS*	CONTACT NUMBER	CIRCUIT	INTERCHANGE POINTS*		TO DCE	FROM DCE
1	SHIELD	--						
2	SI	A-A'	20	RC	C-B'	II		X
3	SPARE		21	SPARE				
4	SD	A-A'	22	SD	B/C-B'	I	X	
5	ST	A-A'	23	ST	B/C-B'	I		X
6	RD	A-A'	24	RD	B/C-B'	I		X
7	RS	A-A'	25	RS	B/C-B'	I	X	
8	RT	A-A'	26	RT	B/C-B'	I		X
9	CS	A-A'	27	CS	B/C-B'	I		X
10	LL	A-A'	28	IS	A-A'	II	X	
11	DM	A-A'	29	DM	B/C-B'	I		X
12	TR	A-A'	30	TR	B/C-B'	I	X	
13	RR	A-A'	31	RR	B/C-B'	I		X
14	RL	A-A'	32	SS	A-A'	II	X	
15	IC	A-A'	33	SQ	A-A'	II		X
16	SF/SR+	A-A'	34	NS	A-A'	II	X	
17	TT	A-A'	35	TT	B/C-B'	I	X	
18	TM	A-A'	36	SB	A-A'	II		X
19	SG	C-C'	37	SC	C-B'	I	X	

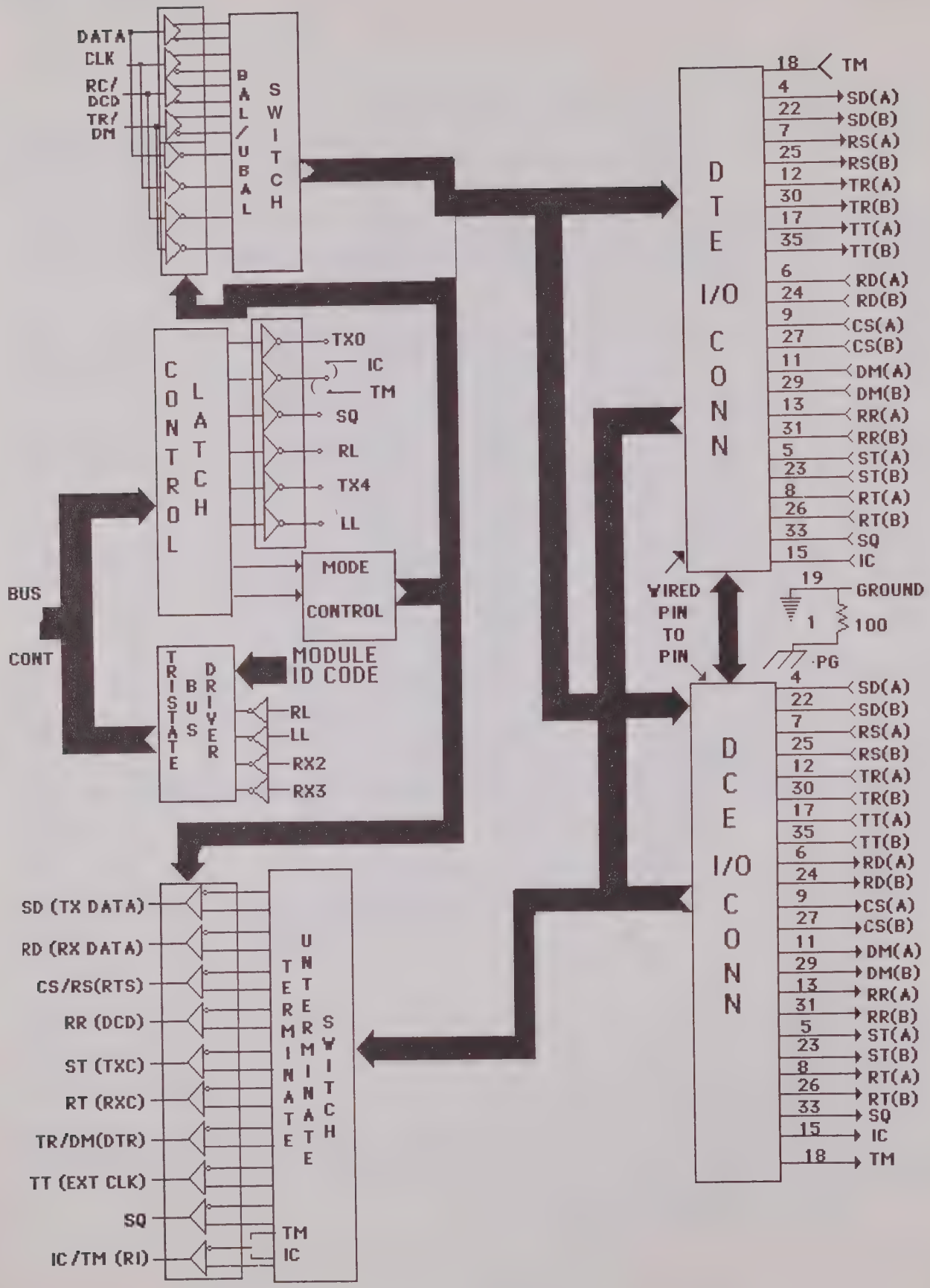


Figure 2-1. RS-449/MIL-188-114 Block Diagram

3.1 REMOTE CONTROL

The Model 450 RS-449 module includes provisions for activating and/or monitoring the status of several special function RS-449 control lines. Because there are no front panel switches to control or indicate status of these functions, the control/monitor capability is provided via the remote control port (RS-232 or IEEE-488) of the Model 5500. The supported functions include Local Loopback, Remote Loopback, Ring Indicator, Test Mode, Signal Quality, 2 spare differential drivers, and one spare TTL receiver (for remote monitoring of any of the TTL level signals on the interface module). Figure 3-2 shows PC board layout for pads referenced in table 3-1.

Table 3-1. Remote Port Control Functions

Remote Control Designation	Model 450 RS-449
TXØ	Spare balanced differential ± 5 volt driver (DTE or DCE mode). Pads on PC board marked "TXØ-A" and "TXØ-B". TXØ-A inverted output, TXØ-B non-inverted output.
TX1	"RI" or "TM" driver (DCE mode). Jumper selectable to "RI" or "TM" on PC board (shipped "RI").
TX2	"SQ" driver (DCE mode).
TX3	"RL" driver (DTE mode).
TX4	Spare balanced differential ±5 volt driver (DTE or DCE mode). Pads on PC board marked "TX4-A" and "TX4-B". TX4-A inverted output, TX4-B non-inverted output.
TX5	"LL" driver (DTE mode).
RXØ	"RL" receiver (DTE or DCE mode).
RX1	"LL" receiver (DTE or DCE mode).
RX2	Spare TTL receiver (DTE or DCE mode). Pad on PC board marked "RX2". May be hard wire jumpered to any TTL signal on the board for sampling via the remote port.
RX3	"SQ" receiver (DTE or DCE mode). Note 1: Resistor R155 (10 ohms) may be removed and RX3 may then be used as a second spare TTL receiver. Pin 8 of U12 is the connect point for the RX3 TTL level test points. Note 2: "SQ" status is indicated by a front panel LED in addition to accessibility via the remote port as RX3. Note 3: "RI/TM" status is indicated by the front panel LED labeled "RI". A jumper on the PC board may be positioned to monitor either "RI' or "TM". (The "RI/TM" status is not accessible via the remote port.)

3.2 TTL TEST SIGNALS

TTL test signals, presented in table 3-2, may be found at the following nodes in the event they are to be jumpered to either the "RX2" TTL receiver or the "RX3" TTL receiver (if R155 is removed).

Table 3-2. TTL Test Signals

TTL Test Signal Node	DTE Function	DCE Function
U13-3	SD	SD
U9-13	RD	SD
U10-13	ST	ST
U10-11	RT	RT
U13-13	TT	TT
U9-11	**DM**	**TR**
U9-5	**CS**	**RS**
U9-3	**RR**	**CS**

Note: **Bold** indicates an inverted line.

3.3 REMOTE COMMANDS

The remote port command for TX drivers is as follows:

> TXØ T "Return" (Sets TXØ to logic true)
> TXØ F "Return" (Sets TXØ to logic false)

To determine the current state of a driver, the command is:

> TXØ "Return" (Asks the status of the TXØ driver)
> FALSE (Command response indicates requested status).

To determine the current state of a receiver, the command is:

> RXØ "Return" (Asks status of RXØ receiver).

> TRUE (Command response indicates requested status).

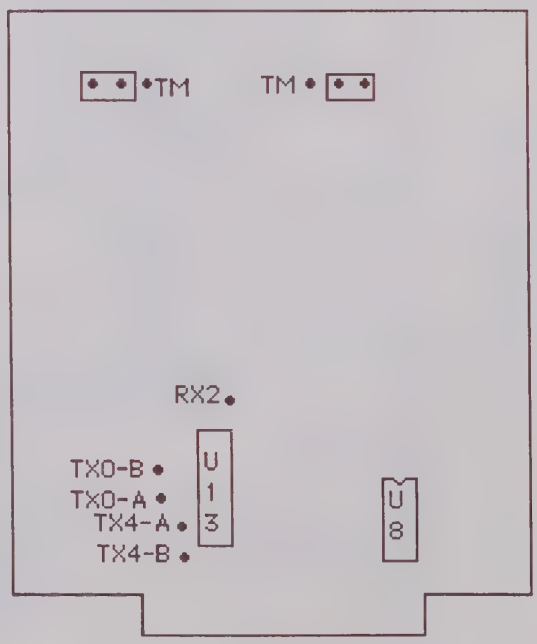


Figure 3-2. PC Board Layout

Model 5500-500

TTL Interface Module

1.0 INTRODUCTION

The Model 5500-500 TTL Interface Module has the same physical connectors and pin assignments as the standard EIA RS-232 25 pin interface; however, the logic is inverted on all data, clock and control lines (relative to standard EIA RS-232 logic convention). DCE or DTE emulation and SYNC or ASYNC mode operation are controlled and switchable from the Model 5500 front panel keys or by commands over the remote ports. The function and operation of this module is identical to that of the Model 5500-200 RS-232 Interface Module, except for the use of TTL gates and logic inversion on all I/O lines.

2.0 DESCRIPTION

Table 2-1 presents the Model 5500-500 TTL Interface Module specifications.

Table 2-1. Model 5500-500 Specifications

CHARACTERISTIC	SPECIFICATION
Modes	Synchronous or Asynchronous
Date Rates	50 bps to 48.0 kbps Asynchronous 50 bps to 4.0 mbps Synchronous
Character Size	5, 6, 7, or 8 data bits
Parity	Odd, Even, or No parity bits
Stop Bits	1 or 2 bits
Input Data Characteristics	MARK signal, binary state 1, or OFF = TTL logic 1.
	SPACE signal, binary state O, or ON = TTL logic O.
Line Drivers	CLK & DATA = "74128" 75 - ohm Drivers
	Control & Status "7408" GATES
Line Receiver	"74HCTO8" GATES

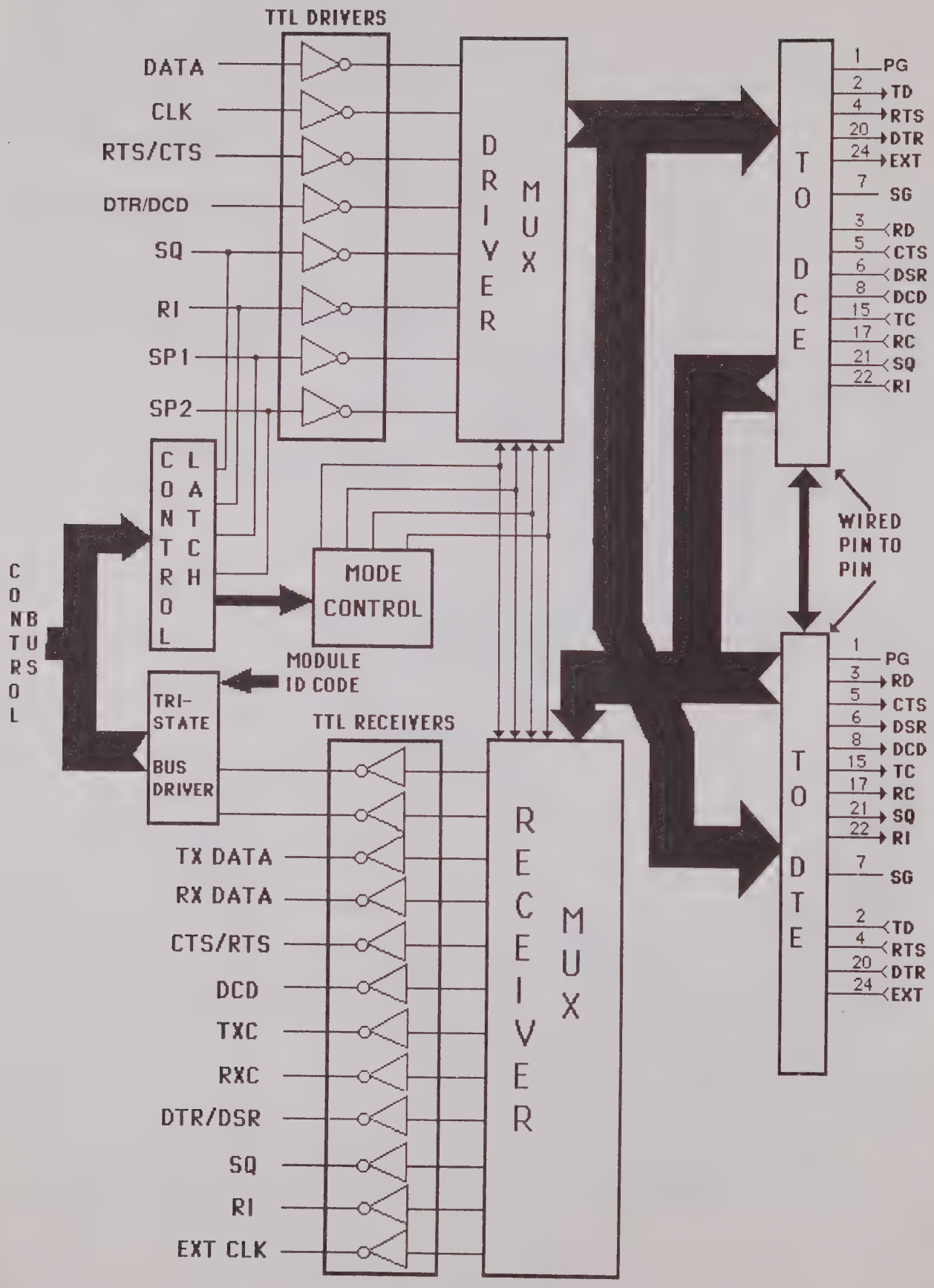


Figure 2-1 TTL Interface Block Diagram

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-500 TTL interface is capable of operation in Synchronous and Asynchronous modes with both DCE and DTE configurations. The module has two 25 pin subminiature 'D' type connectors; Male for DCE and Female for DTE. In addition, the DCE/DTE emulation is electronically switchable from the Model 5500 front panel or via commands over either remote control port. Figure 2-1 presents a simplified block diagram of the Model 5500-200 module.

3.0 OPERATION

3.1 DATA TERMINAL EQUIPMENT (DTE) CONFIGURATION

The Model 5500 may be configured as Data Terminal Equipment (DTE) for testing data Communications Equipment (DCE) such as Modems, Multiplexers, or other peripheral equipments configured as DCE. This is accomplished by toggling the front panel key labeled 'DCE/DTE' until DTE appears in the upper left hand corner of the BERT CRT display (refer to section 3.2 of this instruction book for location and description of the Model 5500 controls and indicators). In the Synchronous mode of operation the Model 5500 may be set to derive clock from the equipment under test or it may generate the clock internally and provide clock to the equipment under test.

In the Asynchronous mode of operation, data is transmitted and received without a clock. Start and stop bits provide proper decoding of the data bits in each character (byte) sent while timing is extracted from the bit transitions. In Synchronous operation, with the DCE under test acting as the source of timing, the Model 5500 bit rate selection should be set to EXTERNAL. In this position the Model 5500 will derive clock from pin 15 (Transmission Signal Element Timing-DCE Source) of the DTE I/O Connector on the interface module. Transmit data and clock are available on pins 2 and 24 respectively, and receive data and clock are available at pins 3 and 17 respectively.

If a Bit Rate is selected on the Model 5500 then the internal generator of the test set supplies the clock signal to the equipment under test. If the user desires to test at a non-standard bit rate the unit can also be operated with an externally applied USER CLOCK into the rear panel BNC connector with the Model 5500 Bit Rate menu set to USER. The frequency of this externally applied clock is read on the CRT display by scrolling through the frequency selections to the appropriate option-either TC or BR.

In either case the test set ignores signals present on pin 15 of the I/O connector; Transmit data and clock are on pins 2 and 24 and Receive data and clock are on pins 3 and 17, respectively.

When operated in an Asynchronous mode the Model 5500 bit rates are internally generated. The appropriate character size, number of stop bits, and parity must also be selected using the front panel cursor and select keys. In this mode of operation no clock signals are transmitted. Transmit data appears on pin 2 and receive data on pin 15 and 17 are ignored. The Model 5500 recovers clock from the received data transitions to provide internal synchronization to the received patterns.

3.2 DATA COMMUNICATION EQUIPMENT (DCE) CONFIGURATION

The Model 5500 may also be configured to operate as a DCE by toggling the DCE/DTE front panel key until the DCE indication appears in the upper left hand corner of the CRT display. Again, either synchronous or asynchronous peripherals can be tested as in the DTE configuration.

In synchronous mode, the Model 5500 may derive clock from the DTE under test or supply clock to the equipment from its own internal generator. When set to CLOCK, the Model 5500 receives timing from the DTE Transmit Signal Element Timing on pin 24 of the rear panel DTE I/O connector. The frequency of the external clock is read on the CRT display by scrolling through the frequency selections to XC. Under this condition the Transmit Data on pin 2 and Transmit Signal Element Timing on pin 24 are analyzed by the Model 5500.

The Model 5500 generates Receive Data on pin 3 and Receive Signal Element Timing on pin 17 in accordance with the DTE supplied clock on pin 24.

To have the Model 5500 supply clock for the equipment under test it is necessary to select the desired bit rate instead of EXTERNAL. In this case, the Model 5500 supplies timing to the DTE under test on pin 15 of the I/O connector. The Model 5500 analyzes the Transmit Data on pin 2 and Transmit Signal Timing on pin 15. Receive Data on pin 3 and Receive Signal Element timing on pin 17 are generated from the Model 5500 internal clock source. A user supplied external clock signal into the USER CLOCK BNC jack will cause the Model 5500 to generate data and clock at the externally applied clock rate when the Model 5500 is set to USER on the BIT RATE menu.

Asynchronous DCE mode operation of the Model 5500 requires selection of the ASYNC mode, bit rate, character size, parity, and number of stop bits. Data is generated and received in character format with no clock signals provided.

Timing is derived from the data transitions and the start and stop bits location identifies the data (character) and parity bits to the receiver for proper decoding.

3.3 CONTROLS AND INDICATORS

Front panel keys labeled RTS/DCD and DTR/DSR enable the user to turn RTS and DTR ON and OFF when the Model 5500 is configured as a DTE.

Twelve green LED's provide visual indication of the primary lead status as follows:

Transmit Data	(TD)
Receive Data	(RD)
Transmit Clock	(TC)
Receive Clock	(RC)
Request to Send	(RTS)
Clear to Send	(CTS)
Data Set Ready	(DSR)
Data Terminal Ready	(DTR)
Data Carrier Detect	(DCD)
Ring Indication	(RI)
Signal Quality	(SQ)
Transmit Clock External	(SCTE).

The front panel key labeled DCE/DTE electronically switches the rear panel I/O Connector functions from DCE to DTE and vice versa. This eliminates the need for special cables to use with the TTL interface module. These and any other functions and indications may be accomplished and displayed at a remote terminal using the RS-232 or IEEE-488 remote control ports. Table 3-3 presents the TTL connector pin assignments.

Table 3-3. TTL Connector Pin Assignments

Pin Number	Interchange Circuit	C.C.I.T.T. Equivalent	Description	Gnd	Data		Control		Timing	
					From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	AA	101	Protective Ground	X						
2	BA	103	Transmitted Data			X				
3	BB	104	Received Data		X					
4	CA	105	Request to Send					X		
5	CB	106	Clear to Send				X			
6	CC	107	Data Set Ready				X			
7	AB	102	Signal Ground (Common Return)	X						
8	CF	109	Received Line Signal Detector				X			
9			(Reserved for Data Set Testing)							
10			(Reserved for Data Set Testing)							
11			Unassigned							
12	SCF	122	Sec. Rec'd. Line Signal Detector				X			
13	SCB	121	Sec. Clear to Send				X			
14	SBA	118	Secondary Transmitted Data			X				
15	DB	114	Sig. Element Timing (DCE Source)						X	
16	SBB	119	Secondary Received Data		X					
17	DD	115	Rec. Sig. Element Timing (DCE Source)						X	
18			Unassigned							
19	SCA	120	Secondary Request to Send					X		
20	CD	108.2	Data Terminal Ready					X		
21	CG	110	Signal Quality Detector				X			
22	CE	125	Ring Indicator				X			
23	CH/CI	111/112	Data Signal Rate Selector (DTE/DCE Source)				X	X		
24	DA	113	Xmit. Sig. Element Timing (DTE Source)							X
25			Unassigned							

Module Switching Unit System

Model 5500-555 MSU I/O Control Module

Model 5500-MSU Module Switching Unit

1.0 INTRODUCTION

The Module Switching Unit System provides the capability to select up to 16 interface modules for use with the Model 5500. The system is modular and may be expanded to switch from as few as two modules up to the maximum of 16 via Module Switching Units that switch up to 4 modules each. This capability eliminates the need to change plug-in modules from the rear of the Model 5500 and enables the user to configure up to 16 separate data channels for test by the Model 5500. The MSU system is compatible with all Model 5500 interface modules and the modules may be installed in the MSU system in any combination, type or quantity, up to the maximum of 16.

Two modes of operation are provided by the MSU system. The MANUAL mode allows the user to select any one of up to 16 modules for "on line" operation via pushbutton selection on the front panel of the Model 5500-MSU. The AUTO mode allows the user to remotely select the "on-line" module from the front panel of the Model 5500.

The complete MSU system (refer to Figure 1-1) consists of the Model 5500-555 MSU I/O Control Module, and four Model 5500-MSU Module Switching Units. The Model 5500-555 MSU I/O Control Module plugs into the interface module slot in the rear of the Model 5500 and provides the control functions for the Model 5500-MSU Module Switching Units. Each Model 5500-MSU Module Switching Unit contains switching provisions for four interface modules. Up to four Model 5500-MSU's may be controlled by a Model 5500-555 MSU I/O Control Module to provide expandable switching capability for up to 16 interface modules.

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-MSU Module Switching Unit.

2.1 FUNCTIONAL DESCRIPTION

The complete MSU system provides the user with the capability to switch up to 16 interface modules for "on line" use by the Model 5500. These 16 interface modules can consist of any combination of module types available for the Model 5500. With the MSU system installed, the user can manually select any of the 16 modules via pushbuttons located on the front panels of the Model 5500-MSU Module Switching Units or by automatic selection via the Model 5500 using either the front panel soft keys and display menu or the remote port on the Model 5500.

The Model 5500-555 MSU I/O Control Module (refer to Figure 2-1) provides all of the command and control functions for up to four Model 5500-MSU's. With the selector switch in the MAN position, the MSU I/O Control Module accepts module selection request commands from the module selector pushbuttons located on the front panel of the MSU's, via connector J2. These switch selections are decoded by the internal control logic and a "Module Enable" command is sent to the corresponding MSU to place the selected module "on line". With the selector switch in the AUTO position, module selection can be performed via the Model 5500 (refer to MSU configuration menu in Section 3) in addition to the pushbuttons on the front panel of the MSU's. When performing module selection via the Model 5500, the user selects the desired module from the MSU configuration menu or via the remote port. The Model 5500, in turn, sends a command to the control logic of the MSU I/O Control Module to place the desired module "on line". The MSU I/O Control Module then sends a "Module Enable" command to the corresponding MSU. When performing module selection via MSU front panel pushbuttons, in the AUTO mode, pushbutton selections are passed to the Model 5500 via the MSU I/O Control Module. The Model 5500 then commands the MSU I/O Control Module to enable the selected module as described above. A remote lockout feature is included in the Model 5500 MSU configuration menu that can be enabled to prohibit module selection via the MSU front panel pushbuttons.

Table 2-1. Model 5500-555 Specifications

CHARACTERISTIC	SPECIFICATION
Dimensions:	17.20" W. x 5.25" EIA (5.22") H x 12.79"D
Weight:	18 lbs. (approx.) excluding modules
Power:	Selectable 115/230 VAC ± 12% 47 to 60 Hz. 26W standby, 40W on line (max)
Environmental:	0 to 50 degrees C (operating) -10 to 85 degrees C (storage)
Front Panel Controls, and Indicators:	Module select momentary pushbutton, Module "ON LINE" LED indicators, Chassis 'ON LINE" LED indicators, Chassis ID CODE selection switch, Power ON/OFF LED indicator.
Rear Panel Controls, and signal access:	Power ON/OFF switch controls operation in conjunction with Model 5500. 2-Dual 50 pin ribbon cable jack pairs for daisy-chain configuration.

Once a module has been placed "on line", the MSU system becomes transparent to both the "on line" module and the Model 5500. This transparency remains in effect until a new module is selected. The MSU I/O Control Module as well as the Model 5500-MSU Module Switching Unit contain differential line drivers and receivers to pass all of the Model 5500 module interface signals between the Model 5500 and the "on line" module.

The Model 5500-MSU Module Switching Unit (refer to Figure 2-2) provides the switching capability for four interface modules. Up to four MSU's may be controlled from a single MSU I/O Control Module. Each MSU must be assigned a sequential chassis ID code via the chassis ID code switch on the front panel upon installation. If two MSU's are utilized they must be assigned chassis ID codes 1 and 2 respectively, if four MSU's are utilized, they must be assigned chassis ID codes 1, 2, 3 and 4 and so on. This chassis ID code provides identification of each MSU to be utilized during command sequences. When a "Module Enable" command is sent by the MSU I/O Control Module, each MSU decodes a portion of the command to extract the chassis ID code. If the chassis ID code matches the switch setting, the MSU decodes the remainder of the "Module Enable" command to place the desired module "on line". This is accomplished by enabling corresponding tri-state buffers, a power relay, and an indicator LED to signify which module is "on line". A chassis "ON LINE" LED is illuminated whenever one of the modules in an MSU is "on line".

Expansion of the MSU system (refer to Figure 2-3) from one to four MSU's is accomplished by connecting the MSU's together in a daisy-chain fashion. Terminating adapters, supplied with the Model 5500-555 MSU I/O Control Module must be installed on the last MSU in the chain. The J1A&B connectors are keyed differently than the J2A&B connectors, as are the supplied cables, to prevent interconnection mistakes.

Power to the MSU is controlled via the on/off switch on the rear panel of the MSU in conjunction with the Model 5500. Both the Model 5500 power switch and the MSU power switch must be on to enable power to the MSU system.

The MSU can be configured to operate on either 110 VAC or 230 VAC by removing the top cover and selecting the line voltage via the selector switch on the AC input module.

Modules may be inserted or removed from the MSU with power on, since power is not applied to a module slot until the module is selected. However, the user should take precautions no to insert or remove a module when the module slot is selected, otherwise damage may occur to the module or to the MSU.

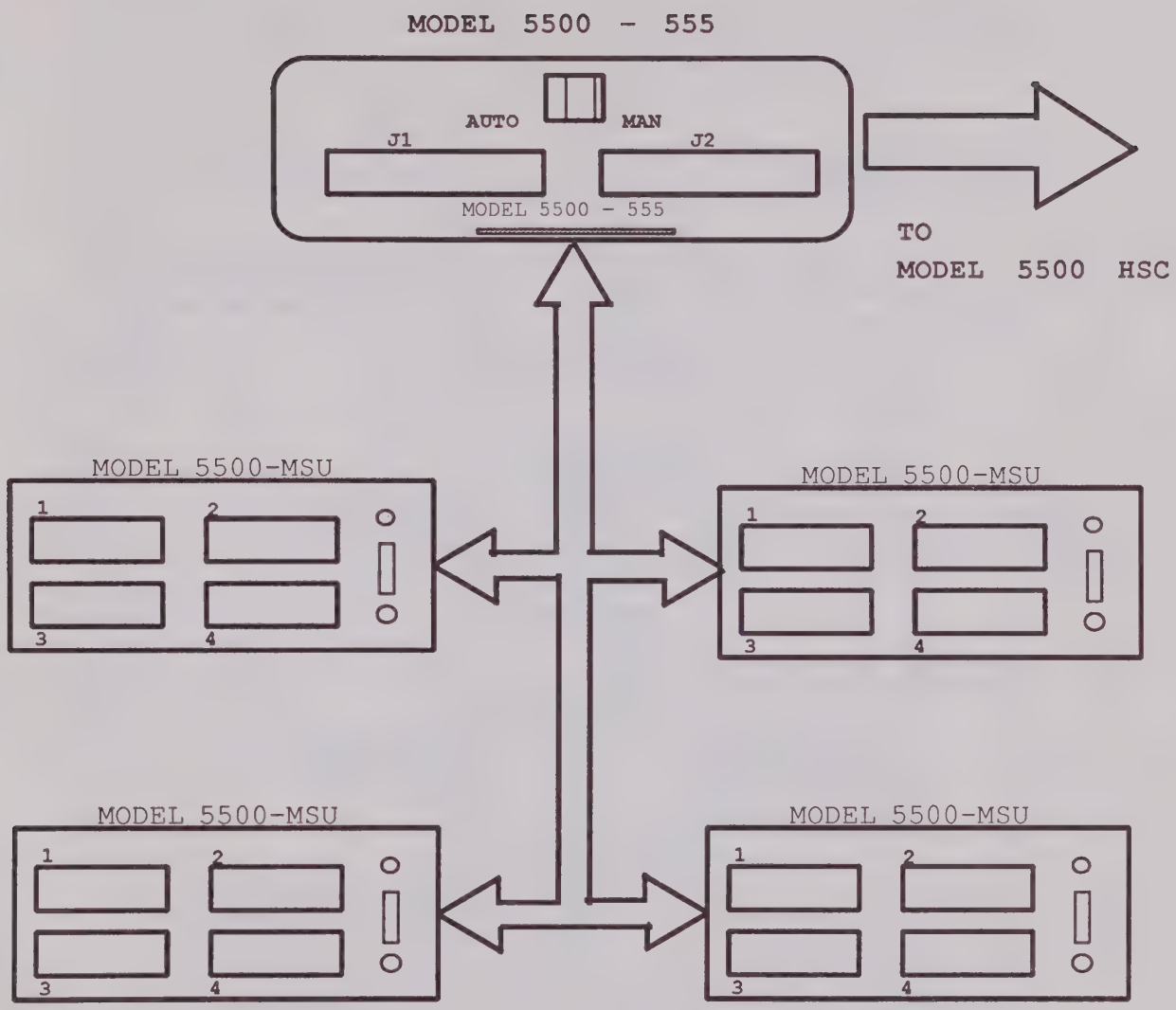


Figure 1-1. MSU System Block Diagram

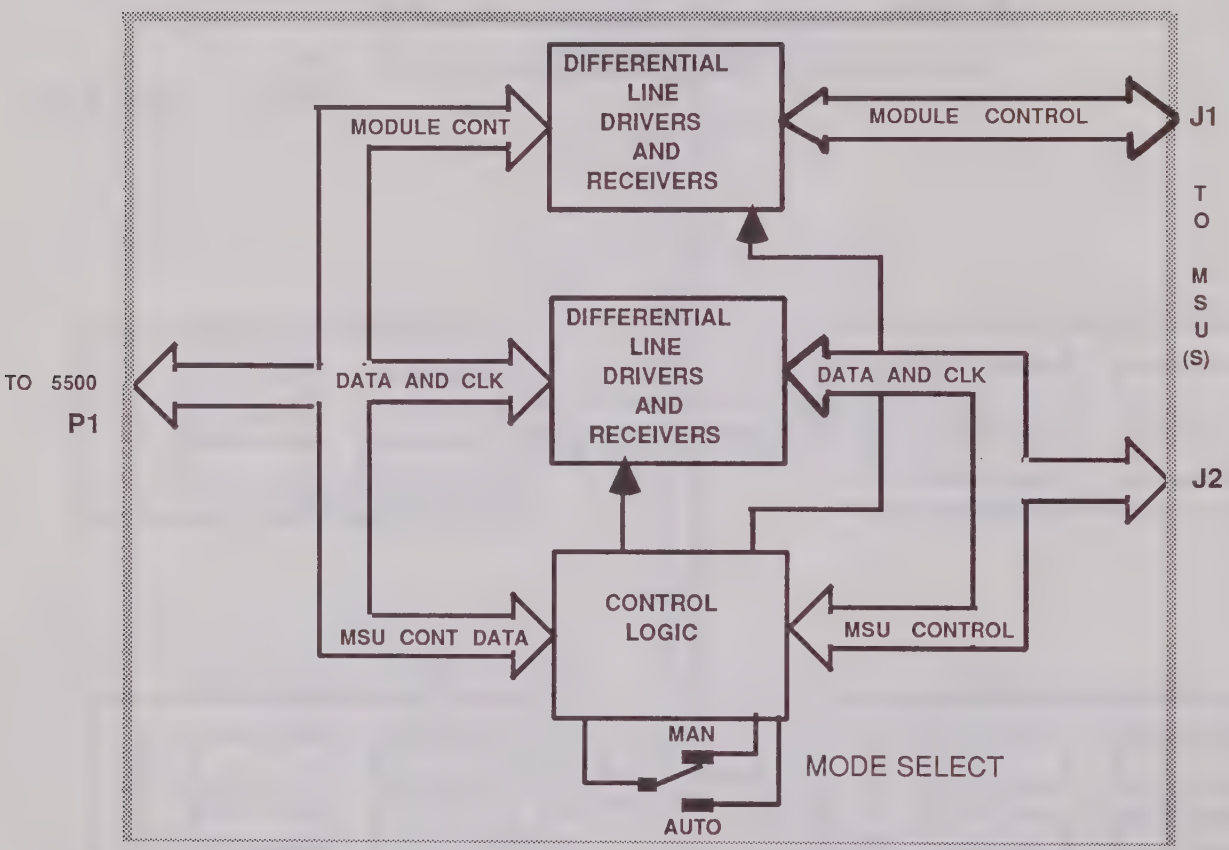


Figure 2-1. Model 5500-555 MSU I/O Control Module Block Diagram

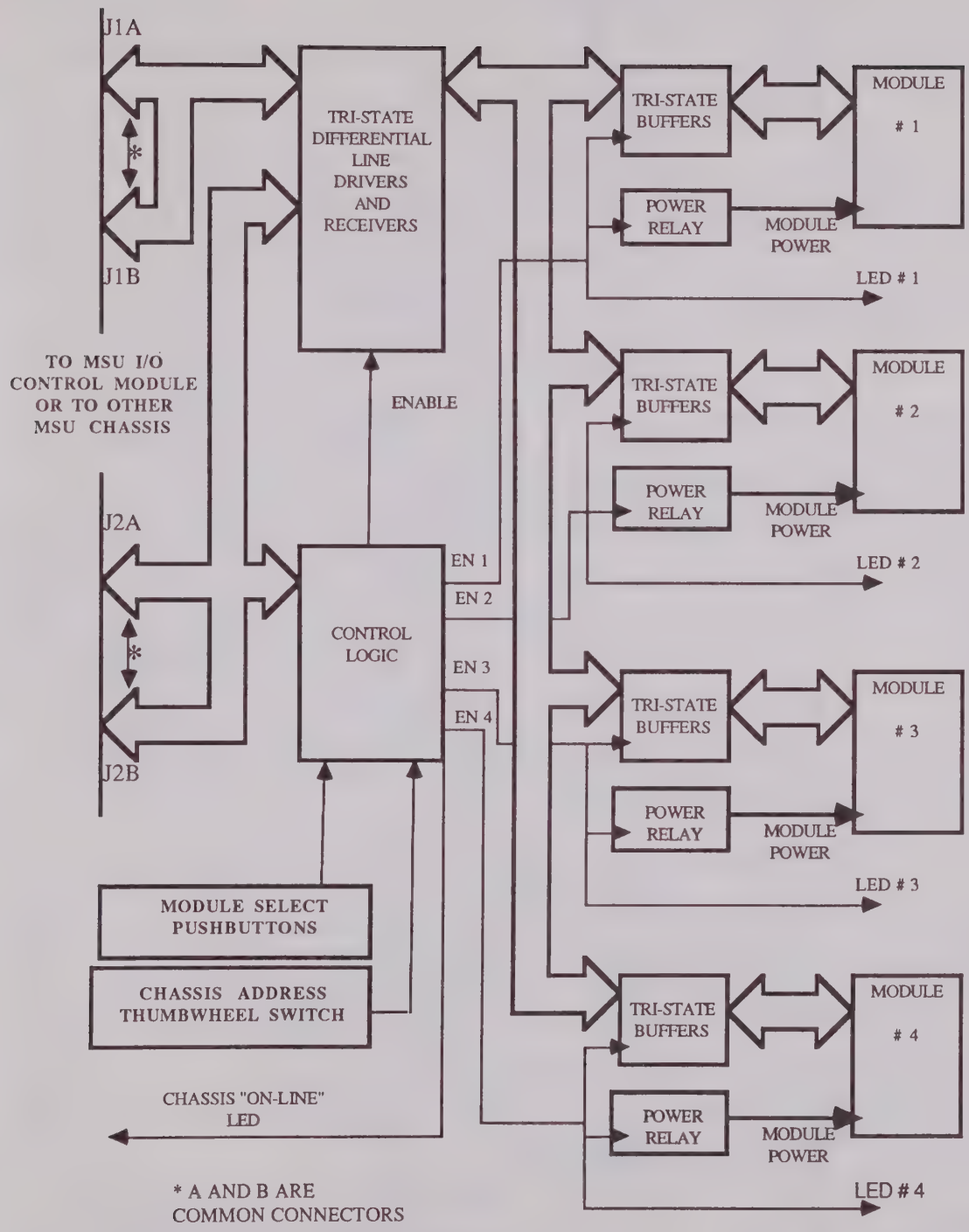


Figure 2-2. Model 5500-MSU Module Switching Unit Block Diagram

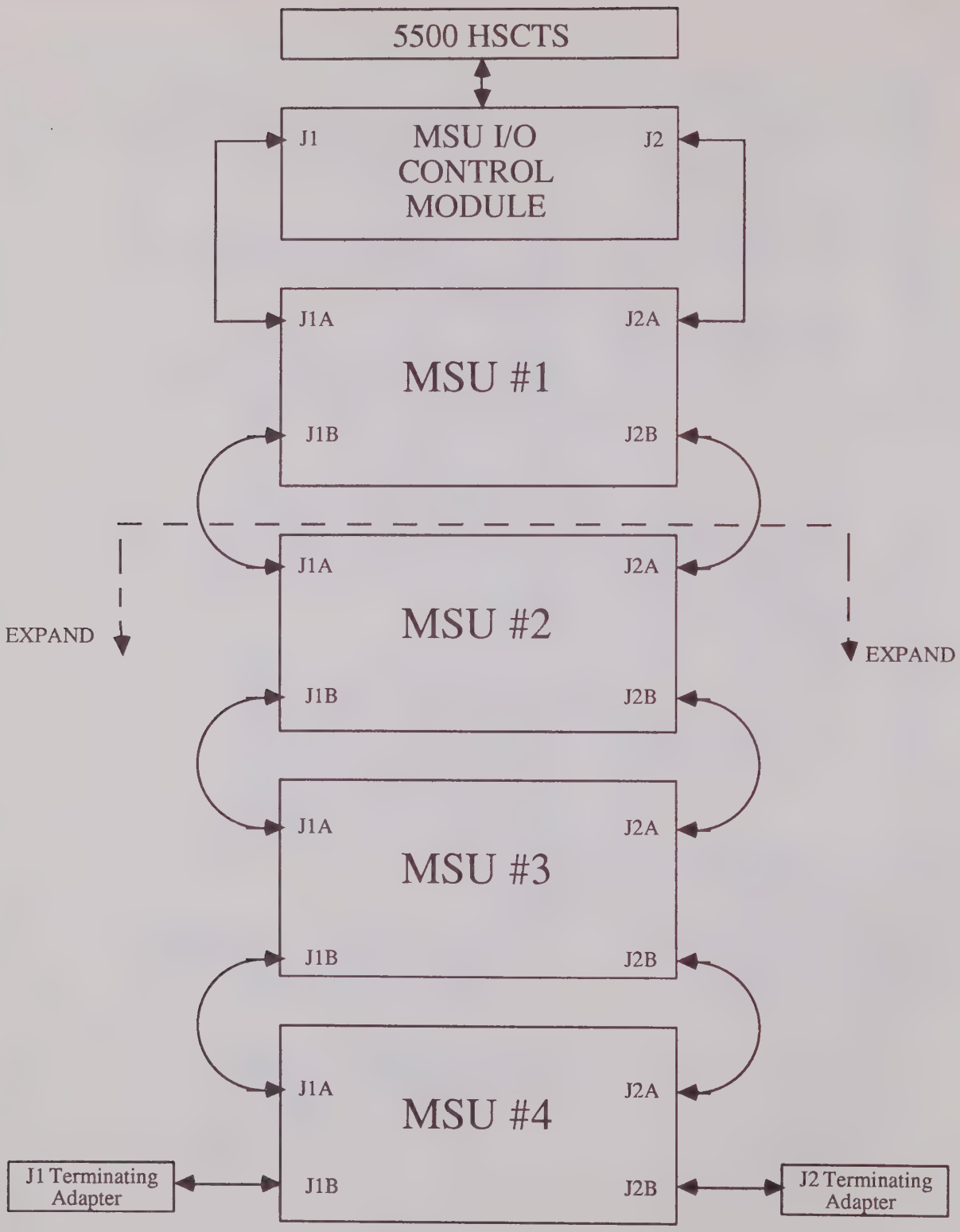


Figure 2-3. MSU System Expansion

3.0 OPERATION

3.1 MSU CONFIGURATION MENU

The MSU Configuration Menu (refer to Figure 3-1) allows the user to control and observe the status of the MSU system via the Model 5500. To select a module, the user moves the cursor to the desired module via the cursor control soft keys and presses either of the two cursor select keys. An asterisk is displayed beside the module to indicate it is "on line" and the module type is displayed at the bottom of the menu. When selecting a module from the MSU front panel pushbuttons, the asterisk will move to indicate the "on line" module as it is selected. The remote lockout feature is enabled or disabled by pressing the adjacent soft keys on the Model 5500 front panel. When a module is selected, a stored operational program must be recalled from the Model 5500 memory (refer to Model 5500 Instruction Book, Section 3 & 4) or the module mode control menus must be reconfigured to place the selected module in the desired mode of operation. Stored programs may also be preassigned to any module slot. To preassign a stored program, the user must position the cursor, via the cursor control soft keys, under the program number column labled "P" and adjacent to the desired module slot. The stored program number may then be assigned by using the hex keypad on the front panel of the Model 5500 or by using the cursor select soft keys. Stored program numbers 0-9 may be assigned directly from the hex keypad or by incrementing or decrementing the program number via the cursor select keys.

Once power is turned on, the Model 5500 interrogates the MSU system to determine module configuration and displays the current MSU configuration on the MSU configuration menu. If a module slot is empty, "empty" will be displayed next to the module slot identification characters. If all four module slots in an MSU are empty, or if the MSU is not installed, "empty" will be displayed next to all four module slot identification characters.

The Model 5500 will then place a module "on line" corresponding to the last module slot "on line" before power off.

3.2 MSU REMOTE PORT OPERATION

Being consistent with other remote port commands, the MSU remote port operation is intended to provide the user with the capability to accomplish any and all of the same functions provided on the MSU menu as well as provide as much helpful information as possible. To accomplish this two remote port commands are used :

INTERFACE and RLOCK

The interface command is not new, but has been modified to include additional information now needed with the MSU system. Both commands if entered as shown above will return the present setting of the respective functions. The interface command will return a line similar to that shown in Figure 3-2, A.

This informs the user that an MSU system is installed, that the card in chassis #1, slot #2 is presently on line, that the card type is and RS-232, and that the program to be recalled upon the selection of this card is program #4.

To obtain a list of the cards presently installed in the MSU system chassis', a query is added to the command :

INTERFACE ?

This returns a list as presented in Figure 3-2, B.

From this list the user may determine which interface he desires to be on line. To change the on line interface enter the command:

INTERFACE xx where xx = chassis#/slot #

For example, to select chassis #1, slot #3 the user would enter the command :

INTERFACE 13

The optional recalled program number associated with each chassis/slot may also be altered. To reassign chassis #1, slot #1 to program #9, enter:

INTERFACE 11 PROGRAM 9

This will alter only the assigned program number and will not affect the on line module. A blank program number indicates that no program is assigned to recalled for that module, leaving off the "9" in the above command would place a blank in the program number space.

The **RLOCK** command was added to the list of remote port commands to allow access to the status of the MSU system remote lockout. The remote lockout disables the effect of the chassis/slot manual pushbuttons when enabled. To determine the present state of the remote lockout, enter:

RLOCK

This will return the state of the remote lockout as either **DISABLED** (manual switches functional) or **ENABLED** (manual switches non-functional). To effect a change in the status the user would follow the RLOCK command with either **ENABLE** or **DISABLE**:

RLOCK ENABLE

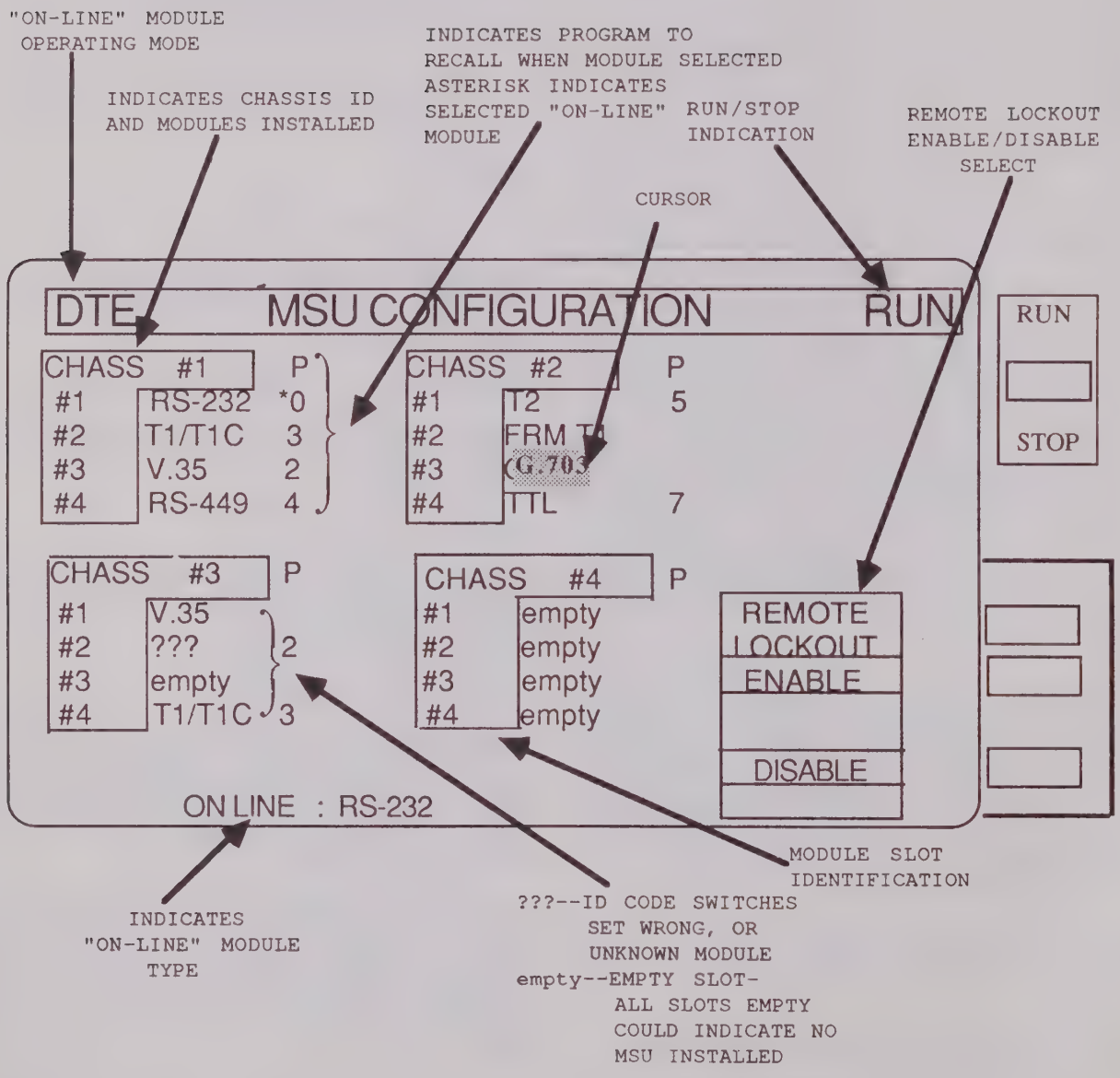


Figure 3-1. MSU Configuration MENU

```
MSU   ( chassis #1 , slot #2 )   CAR   D TYPE : RS-232 ,   PROGRAM 4
```

A

```
MSU   ( chassis #1 , slot #1 )   CAR   D TYPE : V.35    ,   PROGRAM 1
MSU   ( chassis #1 , slot #2 )   CAR   D TYPE : RS-232  ,   PROGRAM 4
MSU   ( chassis #1 , slot #3 )   CAR   D TYPE : T1/T1C  ,   PROGRAM 0
MSU   ( chassis #1 , slot #4 )   CAR   D TYPE : RS-449  ,   PROGRAM 3
MSU   ( chassis #2 , slot #1 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #2 , slot #2 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #2 , slot #3 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #2 , slot #4 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #3 , slot #1 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #3 , slot #2 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #3 , slot #3 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #3 , slot #4 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #4 , slot #1 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #4 , slot #2 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #4 , slot #3 )   CAR   D TYPE : empty   ,   PROGRAM
MSU   ( chassis #4 , slot #4 )   CAR   D TYPE : empty   ,   PROGRAM
```

B

Figure 3-2. Remote Port Responses

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Model 5500-600

DS1/DS1C Interface Module

1.0 INTRODUCTION

The Model 5500-600 DS-1/DS-1C Interface module enables the Model 5500 to test T-Carrier Systems operating at1.544 Mbps (DS-1) and 3.152 Mbps (DS-1C) rates in accordance with the applicable Bell System and U.S. Telephone Association specifications for signals present at the DSX-1 and DSX-1C cross-connect points. The module functions with signals at normal transmit and receive levels as well as with monitor level signals at the DSX points. The T- Carrier signals for T-1 and T-1C systems are serial, bipolar (Return-To-Zero) pulses. The T-Carrier format specifies an Alternate Mark Inversion (AMI) line code limited to no more than 14 consecutive zeroes at T-1. The T-1C signal employs a bipolar AMI signal format where each MARK pulse is opposite in polarity with respect to the previous pulse regardless of how many intervening zeros are present. These Time Division Multiplex (TDM) systems carry twenty four 64 Kbps channels (T1) and forty eight 64 kbps channels (T1C).

2.0 DESCRIPTION

Table 2-1 presents the specifications for the Model 5500-600 DS1/DS1C Interface Module.

Table 2-1. Model 5500-600 Specifications

CHARACTERISTIC	SPECIFICATION
Pulse Rate	T1 - 1.544 Mbps ± 50 ppm Max.
	T1C - 3.152 Mbps ± 50 ppm Max.
Output Pulse Amplitude	T1/T1C + 3.0 V ±10% into 100 ohms
Output Pulse Width	T1 - 324 ±30 nsec at 50 percent amplitude
	T1C - 159 ±20 nsec at 50 percent amplitude
Rise and Fall Times	T1 - 50 nsec ±25 nsec (10-90%)
	T1C - < 50 nsec (20-80%)
Overshoot	Less than 10% of amplitude height.
Receiver Input	Automatic phase compensation for signal levels of 0.8 V peak (-11.5db) to 6.0 V peak (+6db)
Input Impedance	100 ohms ±5% terminated. Greater than 1000 ohms bridged.

2.1 FUNCTIONAL DESCRIPTION

The Model 5500-600 DS1/DS1C Interface Module enables the Model 5500 to generate and receive T1 and T1C serial data streams, recover clock, and regenerate data from low level signals. The mechanical interface between the module and the system under test consists of Western Electric Company type 310 compatible jacks for Transmit and Receive, and a 15 pin subminiature D type connector for Transmit and Receive Data (Used by some Modem and CSU Manufacturers) whose pins are in parallel with the TX and RX 310 jacks (refer to figure 2-1).

The Generator section consists of a line encoder and a line driver. The line encoder produces AMI or B8ZS line code for the bit stream at the T1 rate and AMI line code at T1C rates. This bit stream is then fed to the line driver for transmission. The receive section of the module contains two independent receivers. This configuration enables the Model 5500 to monitor both Receive and Transmit pair traffic for Bipolar Violations. The Receive input has a switchable line termination of 100 ohms. In the BRIDGE mode, both the Transmit and Receive interface circuits are connected to high impedance line receivers with line decoders and bipolar violation detectors. Full BERT functions are provided on the Receive input in BRIDGE mode; BPV and frequency measurement are provided for the Transmit side receiver circuit in BRIDGE mode. The clock recovery circuit (a phase locked loop) derives timing from the incoming bit stream and feeds it to the data detector and line decoder.

The Line Decoder is set to AMI or B8ZS as appropriate and converts the line coded signal to a TTL level bit stream for analysis by the Model 5500 internal logic. The BPV detector compares the output of the Data Detector to the AMI coding rule and passes information on violations of the rule to both the line Decoder, and Counter Timer circuits which in turn initiate the count of BPV's displayed on the CRT.

In the B8ZS mode of operation the Line Decoder and Bipolar Violation Detector combine to ignore intentional Bipolar Violations.

The Model 5500-600 should not be used to test switching equipment or other items requiring a framed T-Carrier signal. For testing such equipments use the Model 5500-624 framed/unframed T1 Module described in the following section. Unframed test patterns are normally used to test inter-office trunks, repeaters, and facility equipment such as multiplexers when coordinated testing is possible and frame alarms can be disabled.

The Model 5500 has a programmable code generator and receiver, and can select AMI or B8ZS operation. The unit can be programmed for other zero substitution type codes, but AMI and B8ZS are the commonly used codes in the U.S. for T-1. T-1C will continue to use an AMI format so far as is known but the Model 5500 can accommodate new formats should this change.

The Model 5500 also has user selectable bit error and bipolar violation injection rates when the Model 5500-600 is installed (refer to figure 3-1). Telephone companies typically employ protection switching for T-Carrier spans and multiplexers. These devices are set to switch to a backup T-Carrier span if the error rate on a working line goes above a predetermined threshold. The usual nominal switching threshold is 1 x 10E-3 violations per bit. To check proper operation of the automatic protection switch (APS) the user can program BPV injection rates slightly above the threshold to ascertain whether or not there are any false triggerings, and that the switch does indeed switch once the threshold has been crossed. For multiplex testing it is also desired to be able to program the bit error rate for setting major and minor alarm thresholds (usually 1 x 10^{-6} and 1 x 10^{-7} errors per bit), and to be able to insert controlled amounts of BPV's which the multiplexers are supposed to correct.

The Quasi-Random Signal Source (QRSS) or Quasi-Random Word (QRW) is a (2^20)-1 pseudo-random sequence which employs >14 zero suppression for T1 testing (telephone industry standard). The (2^20)-1 pattern (without >14 zero suppression) has a natural 19 zero limit and is the standard pattern for T1-C testing.

In addition to the QRW and (2^20)-1 patterns, other patterns are available, or can be programmed in by the user for special cases. Selectable patterns include the Set and Reset codes to loopback and reset T1 Channel Service Units (CSU). The Model 5500 can also send ALL1's pattern (MARK) pattern), which is the "BLUE" signal for DS1 and DS-1C. Up to 135 characters (1080 bits) may be programmed into the USER PATTERN using the front panel HEX keypad, or a remote terminal.

3.0 OPERATION

T1 or T1C is selected by placing 2 switches on the T1/T1C interface module in the proper position. (Refer to inset, figure 2-1). Table 3-1 provides T-Carrier BERT Format definitions that are unique to the Model 5500-600 Interface Module.

3.1 BER TEST ASSISTANCE

Table 3-2 presents a list of possible problem areas if the Model 5500 does not achieve synchronization with the device under test.

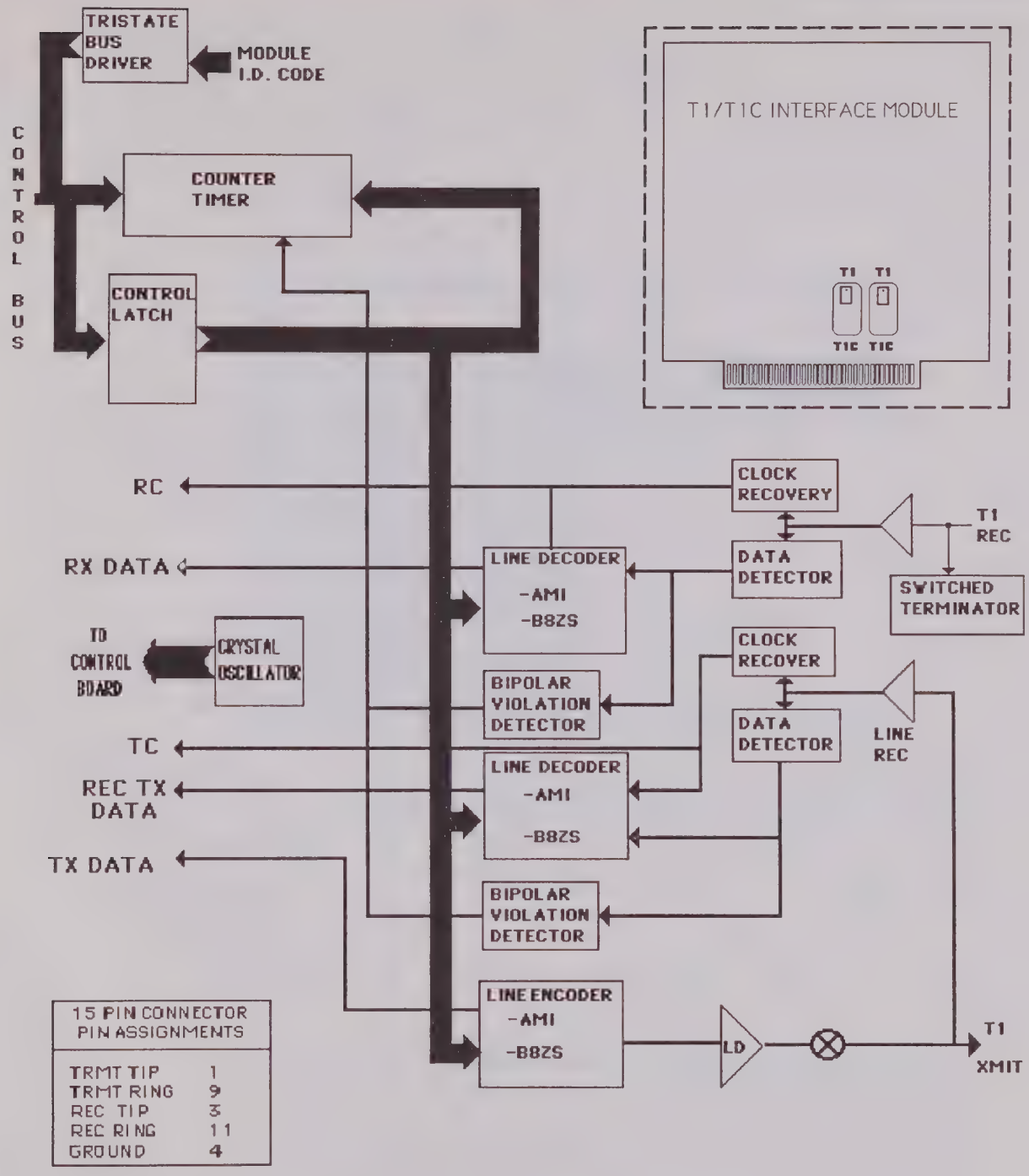


Figure 2-1. Model 5500-600 Interface Module Block Diagram

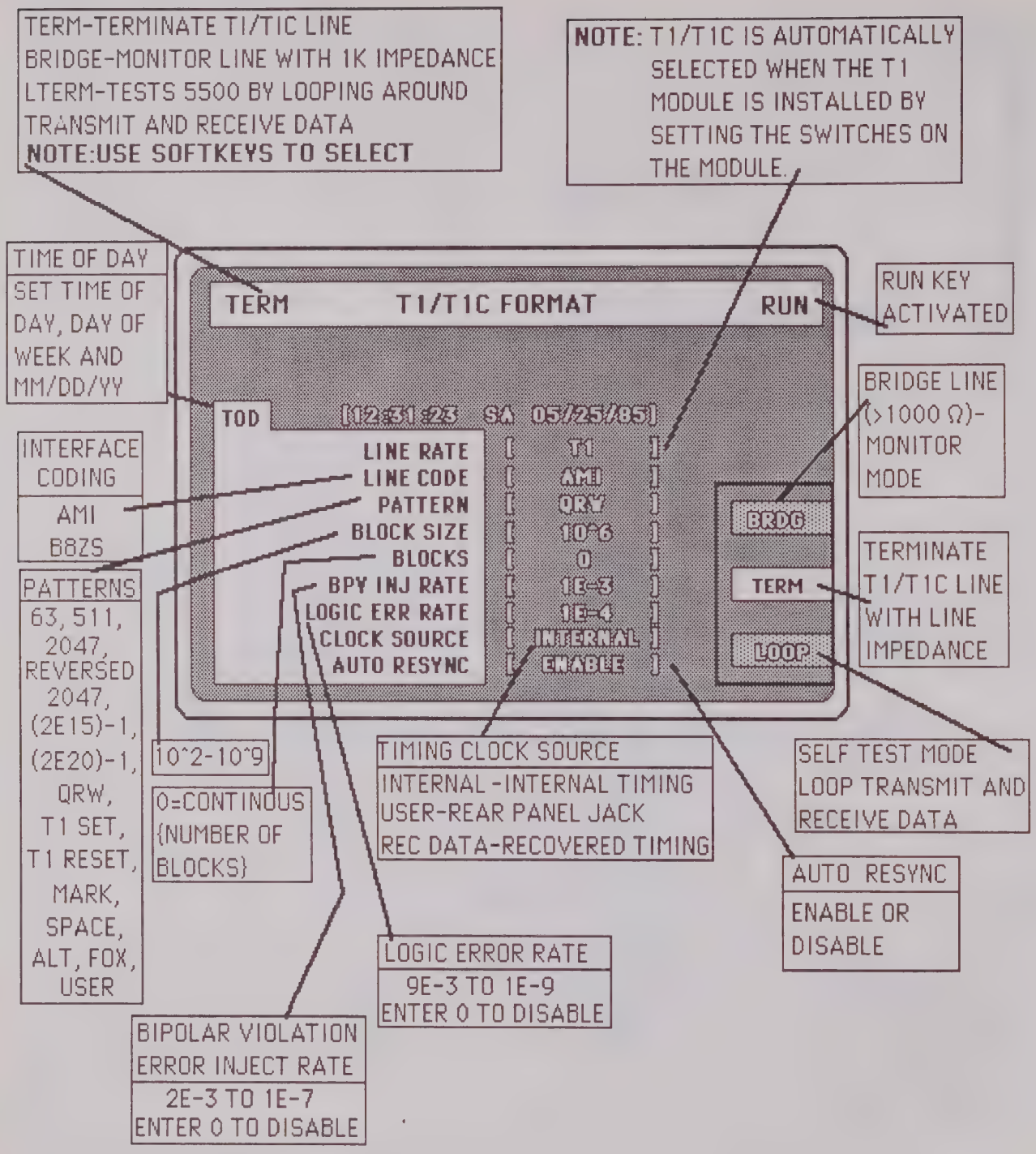

TERM-TERMINATE T1/T1C LINE
BRIDGE-MONITOR LINE WITH 1K IMPEDANCE
LTERM-TESTS 5500 BY LOOPING AROUND
TRANSMIT AND RECEIVE DATA
NOTE:USE SOFTKEYS TO SELECT
NOTE: T1/T1C IS AUTOMATICALLY SELECTED WHEN THE T1 MODULE IS INSTALLED BY SETTING THE SWITCHES ON THE MODULE.
TIME OF DAY
SET TIME OF DAY, DAY OF WEEK AND MM/DD/YY
TERM
T1/T1C FORMAT
RUN
RUN KEY ACTIVATED
TOD
[12:31:23 SA 05/25/85]
LINE RATE [T1]
LINE CODE [AMI]
PATTERN [QRW]
BLOCK SIZE [10^6]
BLOCKS [0]
BPV INJ RATE [1E-3]
LOGIC ERR RATE [1E-4]
CLOCK SOURCE [INTERNAL]
AUTO RESYNC [ENABLE]
BRDG
TERM
LOOP
BRIDGE LINE (>1000 Ω)-MONITOR MODE
TERMINATE T1/T1C LINE WITH LINE IMPEDANCE
INTERFACE CODING
AMI
B8ZS
PATTERNS
63, 511, 2047, REVERSED 2047, (2E15)-1, (2E20)-1, QRW, T1 SET, T1 RESET, MARK, SPACE, ALT, FOX, USER
10^2-10^9
0=CONTINOUS (NUMBER OF BLOCKS)
TIMING CLOCK SOURCE
INTERNAL -INTERNAL TIMING
USER-REAR PANEL JACK
REC DATA-RECOVERED TIMING
SELF TEST MODE
LOOP TRANSMIT AND RECEIVE DATA
AUTO RESYNC
ENABLE OR DISABLE
LOGIC ERROR RATE
9E-3 TO 1E-9
ENTER 0 TO DISABLE
BIPOLAR VIOLATION ERROR INJECT RATE
2E-3 TO 1E-7
ENTER 0 TO DISABLE

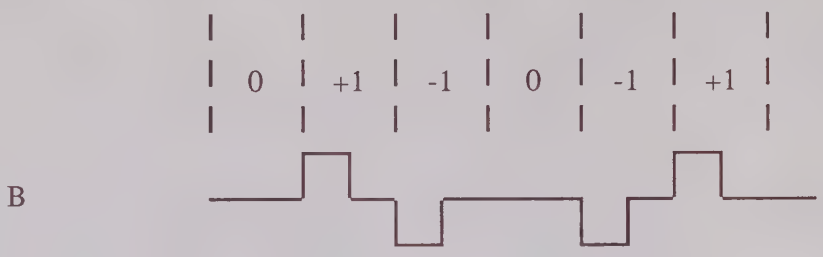
Figure 3-1. T1 BERT Format

Table 3-1. BERT Format Definitions

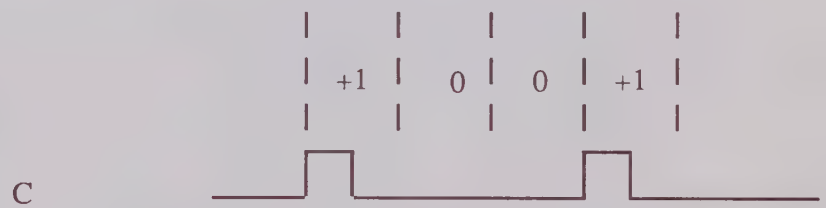
ITEM	DEFINITION
LINE RATE	This block displays the line rate as T1, T1C, or T2 for U.S. systems or 2.048 and 8.448 Mbps for CCITT G.703 modules. This is not a selectable parameter but is fixed by the interface module inserted into the Model 5500. It is a convenience item to remind the operator of the rate at which the Model 5500 is testing.
LINE CODE	The line code of the T-Carrier system under test may be selected by moving the half intensity block over the LINE CODE window and using the SELECT keys to choose the options. The options are: T1 AMI or B8ZS T1C AMI or B8ZS T2 AMI or B6ZS 2.048 Mbps AMI or HDB3 * * 2.048 Mbps G.703 modules are set for HDB3 at the factory. A DIP switch on the module allows selection of AMI coding. The Alternate Mark Inversion (AMI) or Bipolar line code is the line code currently in use in the U.S. on all T1 baseband source code into AMI line code. Note that successive MARKS (1's) always alternate in polarity. A new format, Bipolar 8 Zero Substitution (B8ZS), is being considered for T1 in order to remove the restrictions on the number of successive SPACES (0's) which AMI places on the source coder. While not in actual use at the present time, this line code may become the future standard. An example of a B8ZS coded signal is provided in figure A. Assuming the last 1 transmitted was a positive "one". The polarities of the substituted word are simply reversed if the last "one was negative. 0 0 0 0 0 0 0 0 original word 0 0 0 +1 -1 0 -1 +1 substituted word BPV's always occur at the 4th and 7th bit positions of the substituted word. The line code used by T2 carrier systems is B6ZS which is similar to the B8ZS code previously discussed but which limits strings of 0's to less than 6. In this case a block of six consecutive zeros is substituted by the sequence "0 + - 0 - +" if the preceding mark was positive, or "0 - + 0 + -" if the preceding mark was negative (+ or - represents a positive or negative mark). An example of B6ZS coding is shown in figure B.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION



Finally, High Density, Bipolar 3 Zero Substitution (HDB3) line coding is used in European T-Carrier systems at 2.048 MBPS and 8.448 MBPS line rates. An example of this coding format is shown if figures C and D. (Preceding violation was negative and preceding pulse was negative in figure C and the preceding violation was negative and the preceding pulse was positve in figure D.)



The HDB3 coding process generates positive and negative marks alternately each time a binary logical 1 condition occurs within the message signal. However, unlike AMI coding, the maximum number of consecutive zeros is limited to a value of 3. If a series of 4 consecutive zeros does occur, the 4th zero is replaced by a mark referred to as a VIOLATION. The violation mark is always inserted with the same polarity as the preceding mark. This identifies the departure from the AMI scheme and indicates the occurrence of the violation.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
	In theory, if additional safeguards were not taken, it would be possible for several violations to have an identical polarity, and thus introduce a DC component into the signal. To overcome this problem, the coder continuously monitors the polarity of the last violation (may have been many bits earlier in the data stream) and the polarity of the last mark. The coder then forces the first bit of the 4-bit substitution sequence to a one or a zero, whichever is required, to allow the violation in the fourth bit position to be of opposite polarity to the previous violation.
PATTERN	The pattern choices from the regular FORMAT are all present in T-Carrier FORMAT, but the most useful patterns for T-Carrier testing are:
QRW QUASI-RANDOM WORD	A pattern of (2^20)-1 bits long which has built-in suppression of strings of 0's greater than 14. This pattern is the industry standard for T1 and T1C testing. (2^15)-1: A pseudo-random sequence used in European CCITT G.703 BER testing and jitter testing. (2^20)-1: A pseudo-random sequence of the same length as the QRW, but without the 14 zero suppression. Useful at T2 and for CCITT testing.
MARK	An all 1's pattern which may be used to simulate the "idle" pattern sent out by digital channel banks in an alarm condition.
USER	This is a user definable pattern of up to 135 characters (1080 bits) which could be used to send out patterns with more than 14 zeros or any other pattern a user may want to transmit.
T1 SET	This pattern sends out the standard T1 Channel Service Unit (CSU) loopback code (10000) to cause a remote CSU to loopback for test purposes. This code should be transmitted for 5 seconds before the CSU will loopback to prevent false loopbacks.
T1 RESET	This pattern sends out the standard T1 CSU reset code to return a CSU in loopback to normal operation. The code (100) should be sent out for 5 seconds to reset CSU loopback.
BPV INJ RATE	The user may select any rate of injection of Bipolar Violations from 2x10-3 to $1x10^{-7}$ violation/bit. The rate is selected by changing the mantissa from 0 to 9 (a 0 disables the inject function) first and then moving the half intensity block to the right and changing the exponent from -3 to -7 as desired. The select keys or the HEX keypad can be used. A common rate is 1x10-3 which is useful in checking automatic protection switches. Pressing the INJ soft key on the main BERT display activates BPV Injection unless there is a "0" in the BPV inject rate mantissa.
LOGIC ERR RATE	Logic errors are what telephone companies call bit errors to distinguish them from BPV's. This rate of bit error injection is selectable from 9x10-3 to 1x10-9 errors/bit. The errors (and bipolar violations) are uniformly spaced throughout the bit stream when the INJ soft key is pressed. Note that the user is free to have either logic errors or BPV's or both injected.

Table 3-1. BERT Format Definitions (Cont)

ITEM	DEFINITION
CLOCK SOURCE	The user may select from three alternatives depending upon what simulation is being attempted. When the Model 5500 is acting as the generator of the T- Carrier it is normal to choose INTERNAL timing so that the Model 5500 is the master clock. This would be the case whenever any loopback testing is performed. The "RX" or Receive Clock choice allows the user to operate a 5500 in what is called a loop timed mode. That is, the Model 5500 derives clock from the received bit stream and uses this to time its transmitter. This is useful if, for example, the user is making an end to end bit error test with Model 5500's at each end. In this case one of the test sets should be on INTERNAL (acting as the master clock) and the other should be set to RX. The final option available is USER which allows the operator to supply a TTL clock to the rear panel BNC connector. The clock supplied must be at the nominal bit rate of the module being used (i.e. 1.544 MHZ for T1 module, 6.312 MHZ for T2, etc..), and should be at least ±30ppm accurate.

Table 3-2. BER Test Assistance

SYMPTOM	POSSIBLE CAUSE
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Verify that BRIDGE mode in T- Carrier testing has not been selected. (BRIDGE mode disables the Model 5500 transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units.
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.
Test suddenly stops and RUN LED goes off	If continuous testing is desired verify that '0' has been placed in the Number of Blocks test window and press RUN. If testing a specific number of blocks verify that the number of blocks selected has been reached when test set stops. This is normal operation.
Model 5500 display errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. NOTE: T1 carrier systems are only specified to provide a 1x10-6 error/bit rate which is about three errors or less every two seconds.

Model 5501

G.821 Performance Evaluation

1.0 INTRODUCTION

Installation of the G821 performance evaluation package changes the designation of the Phoenix Model 5500 to the Phoenix Model 5501. This option allows the operator to monitor the performance of the equipment being tested in accordance with CCITT Recommendation G.821. These measurements are based on time. The total time of the test is divided into increments of time by breaks. A break is defined as a period, measured in seconds, which begins with ten consecutive seconds that are characterized by an error ratio greater than the established threshold (STHR). These errored seconds are referred to as severely errored seconds (SES). A break ends when there have been ten consecutive non-severely errored seconds. This is illustrated in figure 1-1. The period of time, from the first of the ten severely errored seconds to the first of the ten non-severely errored seconds, is referred to as unavailable time, or a break (the circuit is also considered non-available at that time.) Subtracting non-available time from total test time results in available time. Thus the G.821 testing period is divided into available and non-available time. The Phoenix Model 5501 has been designed to operate on the basis of the available and non-available time to provide the operator with all of the significant G.821 parameters.

2.0 OPERATION

It is reccommended that sections 2, 3, and 4 of this instruction book be read before beginning G821 testing.

Measurement of the G.821 paramters is accomplished by selecting the G821 display, shown in figure 2-1. The G821 display is located under the BIG BERT display as shown in figure 3-2 of this instruction book. The G.821 parameters and their definitions are presented in table 2-1. Any of the listed parameters may be selected to be diplayed on the G821 display by moving the cursor over the desired location and toggling the SELECT keys until the desired parameter appears (in figure 2-1 the cursor is shown on the location where DAYS has been chosen). The EBPS, STHR, and MTHR parameters are permanently displayed but the operator may select their values by placing the cursor over the appropriate value. The STHR and MTHR values are entered by using the HEX keypad on the front panel, while the EBPS value is entered by scrolling to the desired value using the SELECT keys.

2.1 REMOTE OPERATION

All of the operating functions of the 5501 may be addressed via the remote ports. (see chapter 2, paragraph 2.5 and chapter 3, paragraphs 3.3.5 thru 3.3.7 of this instruction book) Specifically, the list of G821 parameters and commands can be read over the remote port by invoking the '?' command. The displayed fields on the G821 display screen can be modified by means of the GF1 thru GF12 (this relates to the position on the screen, with GF1 being SES in figure 2-1 and GF12 being SOB). ALL of the G821 parameters will be printed if the G821 field on the print menu (figure 2-2) is selected.

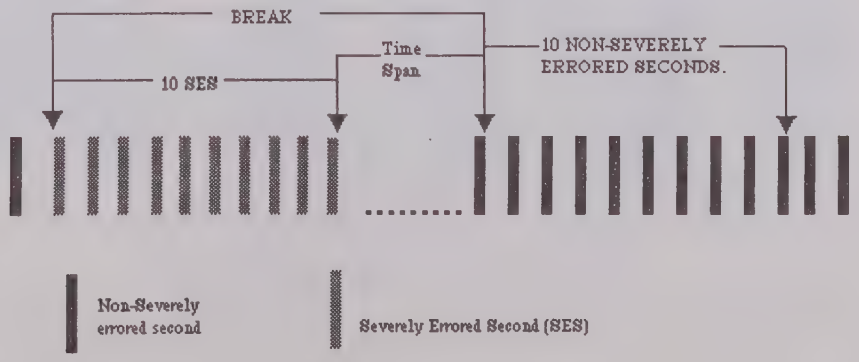


Figure 1-1. G.821 Break

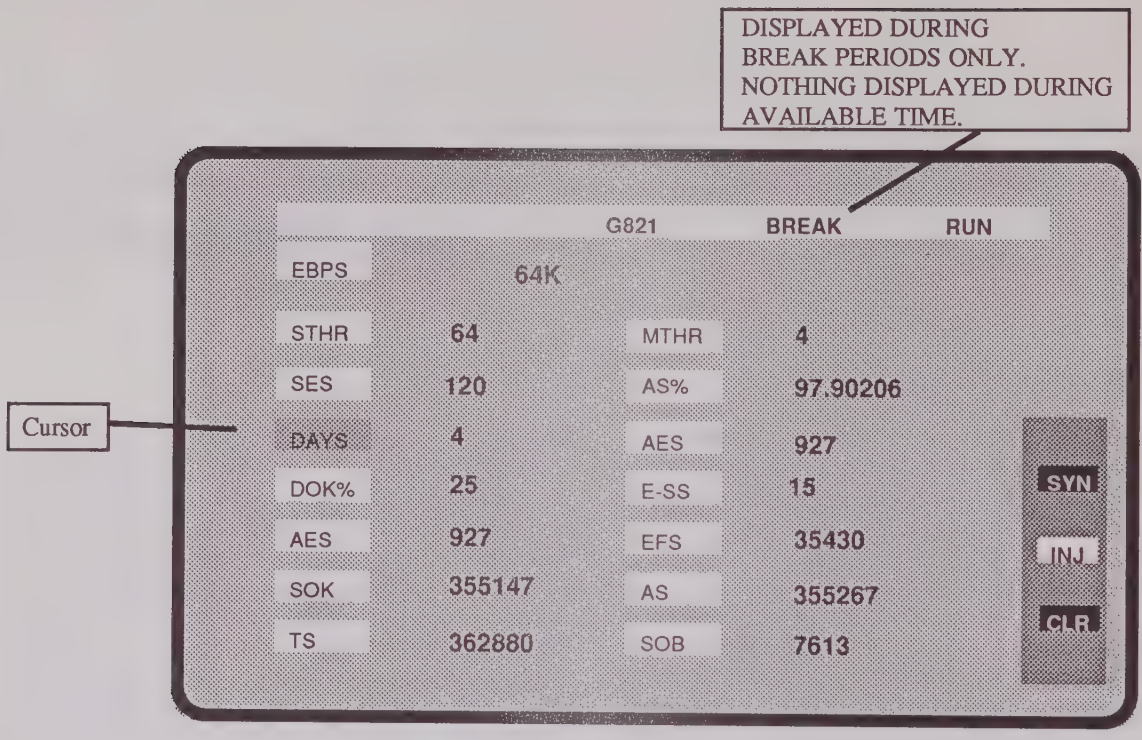


Figure 2-1. BERT G821 Display

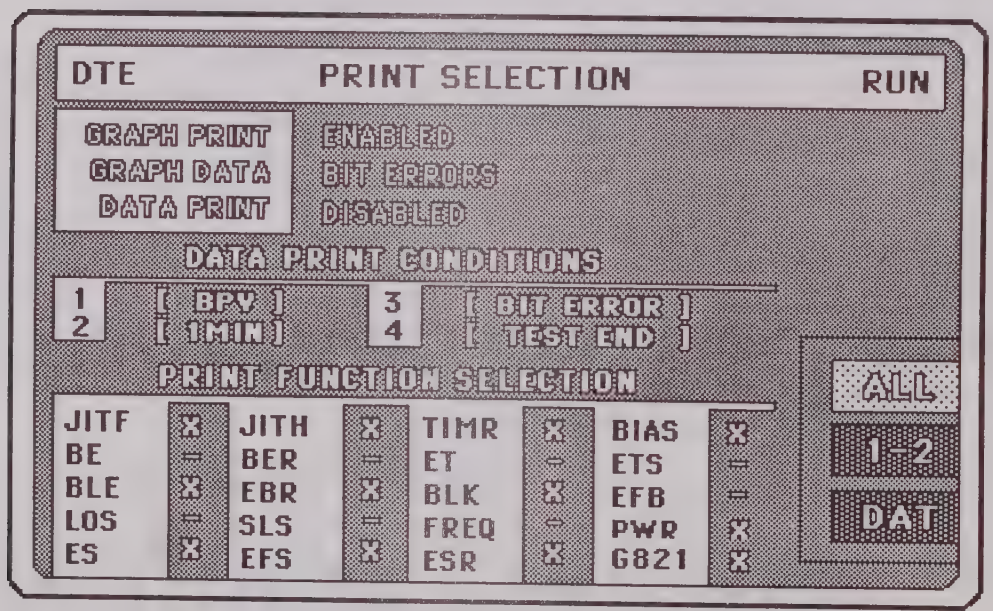


Figure 2-2. BERT Print Menu for Model 5501

Table 2-1. G.821 Parameters

PARAMETER	DEFINITION
TS	Total seconds of test. The accumulation begins when the tester achieves the first synchronization. Subsequent losses/gains of synchronization will not affect the measurement. A test cannot be started on an unavailable circuit.
SES	Severely errored seconds. Seconds that are characterized by a high error ratio. The value specified in the G.821 definition is 10^{-3}, but due to the fact that customers need to be able to set this threshold (STHR) to a lower value, the 5001 allows the operator to specify the number of errors that determines a SES.
SOB	Unavailable seconds (or seconds of break). The sum of every period of unavailable time experienced by the circuit. (Unavailable time is defined in paragraph 1.0.)
MIN	Number of available time minutes. Available time minutes are total minutes less degraded minutes (DM).
DM	Degraded minutes. Available time is divided into packets of sixty seconds, or one minute. The sum of the errors, relative to 60 seconds, is computed and used to characterize the minute. The minute is considered degraded if its total error sum is greater than the threshold (MTHR) that is also programable by the operator. (G.821 defines the error ratio threshold as 10^{-6} which would be 4 at a 64K EBPS)
AS	Available seconds. The sum of every period of available time.
AES	Available errored seconds. The number of seconds, in available time, that are errored.
	* * * * * * * *
	In addition to the above CCITT parameters, the following parameters are also evaluated and available for display. This particuliar set of parameters is primarily intended for testing procedures at British Telecom.
	NOTE: Contact Phoenix Microsystems Customer Service if your needs are not met by these parameters.
EFS	Available error free seconds. The number of seconds, in available time, that are error free. EFS = AS - AES
EFS%	Percent of EFS. The percentage of available error free seconds in relation to the total number of available seconds. EFS% = (EFS/AS) x 100
SOK	Seconds, in available time, characterized by a number of errors less than the selected value of STHR. (G821 spec error ratio as 10^{-3} which is STHR of 64 with EBPS of 64K)
SOK%	Percent of SOK. The percentage of SOK in relation to the total number of available seconds. SOK% = (SOK/AS) x 100
MOK	Minutes, in available time, characterized by a number of errors less than the selected value of MTHR. (G.821 spec error ratio at 10^{-6} which is MTHR of 4 with EBPS of 64K)
MOK%	% of MOK. The percentage of MOK in relation to the total number of minutes. MOK% = (MOK/MIN) x 100

Table 2-1. G.821 Parameters (Cont)

PARAMETER	DEFINITION
AS%	Percent of AS. The percentage of available time in relation to the total test time. AS% = (AS/DAYS) x 100
E-SS	Total number of errors counted during available time, excluding severely errored seconds.
B-SS	Total number of bits received in available time, excluding severely errored seconds.
R-SS	(E-SS)/(B-SS). The error ratio relative to availbale time, excluding severely errored seconds.
NOB	Number of breaks. This counter is incremented any time a new period of unavailable time is detected.
TBFD	Total number of breaks for the day. This counter is reset daily. It is incremented each time a new period of unavailability (break) is detected unless the break crosses the day boundry. In that case, the following rules apply (refer to figure 2-3). 1. A break is always counted for one of the days. 2. If the break lasts for 10 or more seconds in both days, then it is counted in both days.
DAYS	Total number of days of the test.
DOK	Number of break free days. A day of test in which no break has been experienced.
DOK%	Percent of DOK. The percentage of break free days in relation to the total number of days of test. DOK% = (DOK/DAYS) x 100
DB1	The number of days with one break. A day of test in which only one break has been experienced.
DB1%	Percent of DB1. The percentage of days with one break in relation to the total number of days of test. DB1% = (DB1/DAYS) x 100
DB2	The number of days with two or more breaks. A day of test in which two or more breaks occur.
DB2%	Percent of DB2. The percentage of days with two or more breaks in relation to the total number of days of test. DB2% = (DB2/DAYS) x 100
EBPS	Explicit bits per second. This parameter is used to calulate E-SS, B-SS, and R-SS. It is automatically set to the bit rate displayed in the format menu if the clock is generated internally and the interface module is NOT a T-interface. If the clock is an EXTERNAL, user optional, or if a T-interface module is installed, the EBPS value must be entered by the operator. The entry must be the actual bit rate value. Operator entered from front panel or from the remote port.

Table 2-1. G.821 Parameters (Cont)

PARAMETER	DEFINITION
STHR	Severely errored second threshold. This is the minimum number of errors that determine a SES. Operator entered from front panel or from the remote port.
MTHR	Degraded minute threshold. This is the minimum number of errors that determine a DM. Operator entered from front panel or from the remote port.

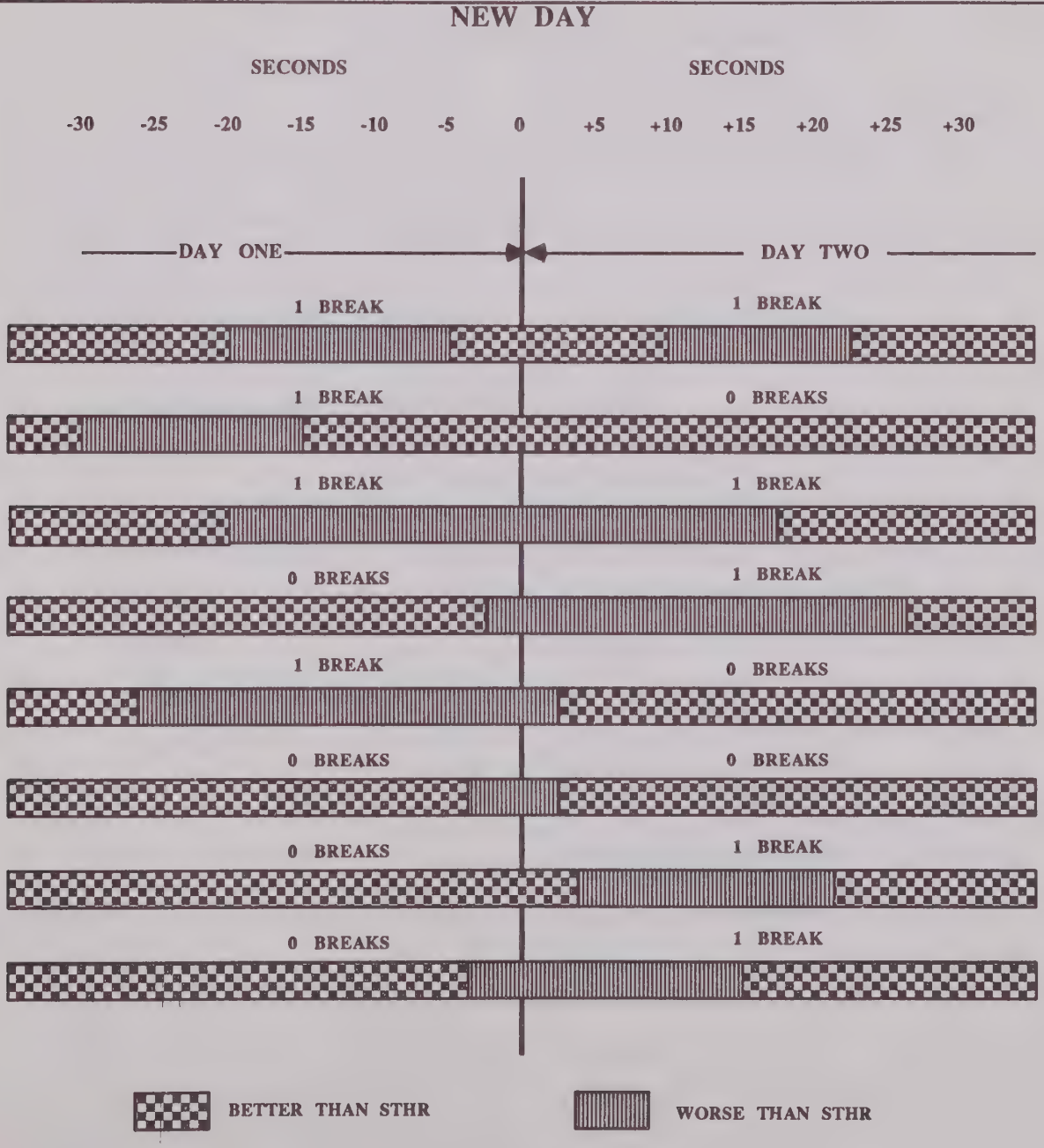


Figure 2-3. Breaks Crossing Day Boundry

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Model 5500-900

303 Bell Interface Module

1.0 INTRODUCTION

This section details the operation of the Bell 303 Interface Module option. ASYNC, SYNC, and External modes are all self contained in the 5500. This module uses much of the same protocol as the RS-232C with minor differences. Two extra control lines were added to give the module loop and mode select capabilities. DCE or DTE emulation, and SYNC, ASYNC or external operations are controlled and switchable from the Model 5500 front panel keys, or by commands over the remote ports.

2.0 DESCRIPTION

Table 2-1 presents the Model 5500 303 Bell Interface Module specifications.

Table 2-1. Model 5500-900 Specifications

CHARACTERISTIC	SPECIFICATION
Modes	SYNC, ASYNC, EXTERNAL
Emulation	DCE or DTE
Data Rates	75 bps to 1.544 Mbps
Character Size	5, 6, 7, 8 data bits
Parity	Odd, Even or no parity bit
Input Data Characteristics	Mark signal, binary state 2, or OFF = -3 Volts min.

2.1 FUNCTIONAL DESCRIPTION

The Bell 303 Interface Module is capable of operation in Synchronous and Asynchronous modes when configured in DTE simulation mode and Asynchronous, Synchronous and External in DCE simulation mode. The module has provisions for 2 types of connectors. A standard subminiature "D" type 15 pin connector and a 25 pin connector commonly associated with Bell System Voiceband Data Sets. The connector is equivalent to a Cinch or Cannon DB-19604-433 connector. The business machine (DTE) should be equipped with a cable not longer than 50 feet and a Cinch or Cannon DB-19604-432 plug mounted in a Cinch DB-51226-1 hood assembly. Figure 2-1 presents a simplified block diagram of the Bell 303 module. Table 2-2 presents the Bell 303 connector pin assignments.

3.0 OPERATION

3.1 DATA TERMINAL EQUIPMENT

The Model 5500 may be configured as Data Terminal Equipment (DTE) for testing Data Communications Equipment (DCE) such as modems, multiplexers, or other peripheral equipments configured in DCE. This is accomplished by toggling the front panel key labeled "DCE/DTE" until DTE appears in the upper left hand corner of the BERT CRT display (refer to section 3.2 of this instruction book for location and description of the Model 5500 controls and indicators). In the synchronous mode of operation the Model 5500 may be set to derive clock from the equipment under test or it may generate the clock internally and provide it to the equipment under test. The ALT Line is set by the DTE and sent to the DCE under test. This sets the DCE to the proper format to receive data. In this case it will expect the data to be sent in the Synchronous mode.

In the Asynchronous mode of operation data is transmitted and received without a clock; start and stop bits provide proper decoding of the data bits in each character (byte) sent, while timing is extracted from the bit transition. In Synchronous operation, with the DCE under test acting as the source of timing, the Model 5500 bit rate should be set to EXTERNAL. In this position the Model 5500 will derive clock from Pin J of the DCE I/O connector on the interface module. Transmit data and clock are available on pins E and H respectively, and receive data and clock are available on, pins K and L respectively.

If a bit rate is selected on the Model 5500 then the internal generator of the 5500 supplies the clock signal to the equipment under test. If the user desires to test a non-standard bit rate the unit can also be operated with an externally applied USER CLOCK. This clock is connected to the rear panel BNC connector with the Model 5500 Bit Rate field set to USER. The frequency of this externally applied clock is read on the CRT display by scrolling through the frequency selections to the appropriate option - either TC or BR. In either case the test set ignores the signals present on pin J of the I/O connector. Transmit data and clock are on pins E and H. Receive data and clock are on pins K and L, respectively.

When operated in an Asynchronous mode the Model 5500 bit rates are internally generated. The appropriate character size, number of stop bits, and parity must also be set using the front panel cursor and select keys. In this mode of operation no clock signals are transmitted. Transmit data appears on pins E and receive data on pin K of the I/O connectors. Any signals appearing on pins J and L are ignored. The Model 5500 recovers clock from the received data transitions to provide internal synchronization to the received patterns.

In the "Bell 303 Format" menu LOOP mode appears in the last row. This mode reflects one of two loop modes associated with this module. The "Selftest" loop mode is the normal loop mode. The "Remote" loop mode sets the loop line on the module and sends it to the DCE with instructions to loop the data back to the sender. This is a data verification technique used for analysis of random data.

3.1.1 Controls and Indicators

Model 5500 front panel controls labeled RTS/DCD and DTR/DSR enable the user to turn RTS and DTR ON and OFF when the Model 5500 is configured as DTE.

Twleve green LED's provide visual indication of the primary lead status as follows:

Transmit Data - (TD)	Data Set Ready (DSR)
Receive Data - (RD)	Data Terminal Ready (DTR)
Transmit Clock - (TC)	Data Carrier Detect - (DCD)
Receive Clock - (RC)	Ring Indicator - (RI)
Request to Send - (RTS)	Signal Quality - (SQ)
Clear to Sent - (CTS)	Transmit Clock Ext - (SCTE)

Table 2-2. Bell 303 Connector Pin Assignments

DTE Pin Number	DCE Pin Number	Interchange Circuit	C.C.I.T.T. Equivalent	Description	Gnd	Data		Control		Timing	
						From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
X		AA	101	Protective Ground (connector body)	X						
E	4	BA	103	Transmitted Data			X				
K	1	BB	104	Received Data		X					
D	5	CA	105	Request to Send					X		
C	10	CB	106	Clear to Send				X			
F"C"	8	CC	107	Data Set Ready				X			
"O"	6	AB	102	Signal Ground (Common Return)	X						
B	14	CF	109	Received Line Signal Detector (Spare)				X			
G	15			Local Test					X		
A	13	SCB	121	Alternate					X		
I	3	DB	114	Sig. Element Timing (DCE Source)						X	
L	2	DD	115	Rec. Sig. Element Timing (DCE						X	
				Source)							
M"O"	12	CD	108.2						X		
M"C"	9	CG	110	Data Terminal Ready				X			
F"O"	11	CE	125	Signal Quality Detector				X			
				Ring Indicator							
H	7	DA	113								X

"C" = center conductor "O" = outer conductor

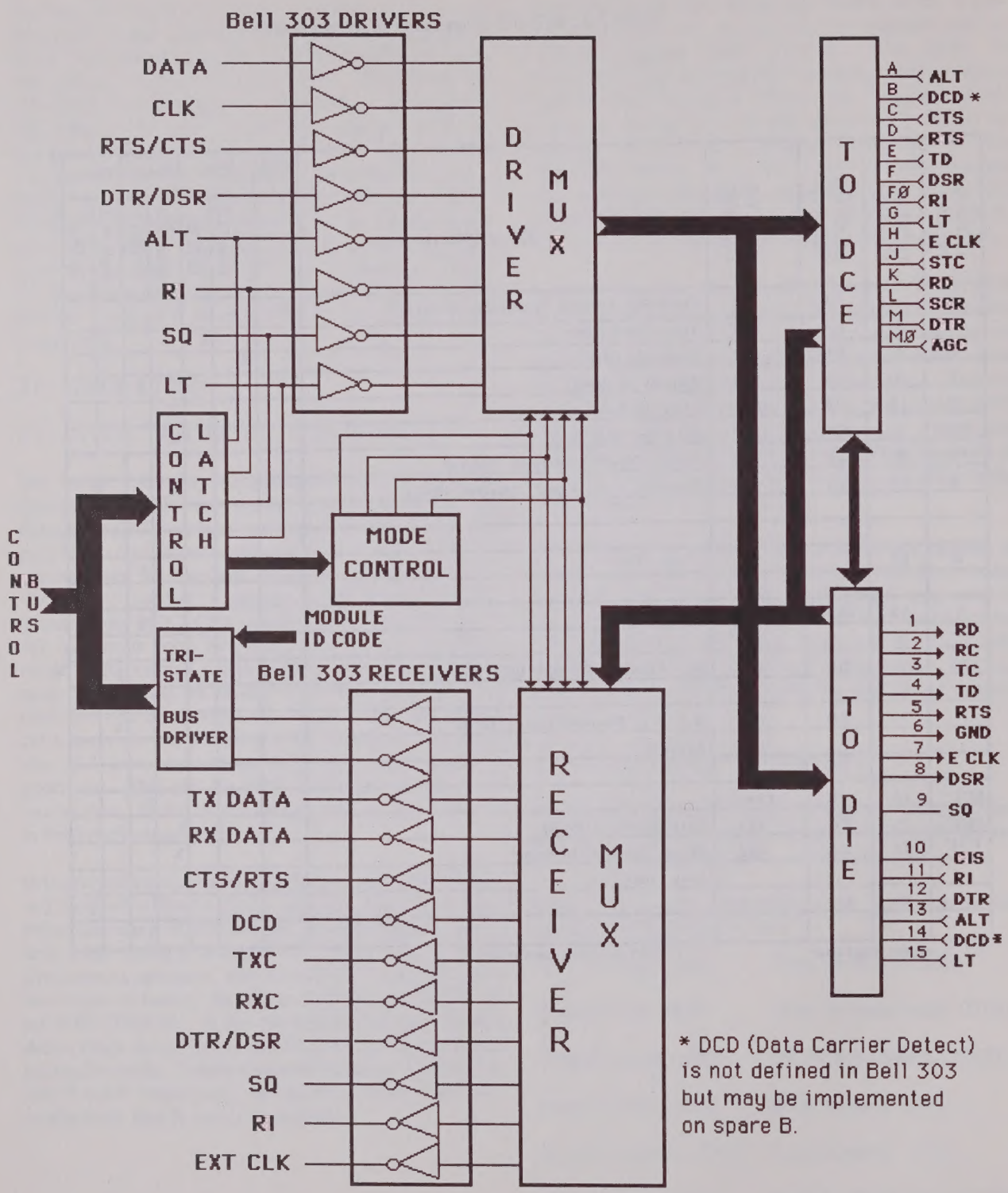

Figure 2-1. Model 5500-900 Interface Module Block Diagram

The front panel key labled DCE/DTE electronically switches the rear panel I/O connector functions from DCE to DTE and vice versa. These and any other function, and indications may accomplished and displayed at a remote terminal using the RS-232 or IEEE-488 remote control ports.

3.2 DATA COMMUNICATIONS EQUIPMENT (DCE) CONFIGURATION

The Model 5500 may also be configured to operate as a DCE by toggling the DCE/DTE front panel key until the DCE indication appears in the upper left hand corner of the CRT display. Again, either Synchronous or Asynchronous peripherals can be tested as in the DTE configuration.

In Synchronous mode, the Model 5500 may derive clock from the DTE under test or supply clock to the equipment from its own internal generator. When set to external clock, the Model 5500 receives timing from the DTE transmit signal element timing on pin 7 of the rear panel DTE I/O connector.

The frequency of the external clock is read on the CRT display by scrolling through the frequency selections to XC. Under this condition the TD on pin 4 and EXTC on pin 7 are analyzed by the Model 5500.

The Model 5500 generates RD on pin 1 and RC on pin 2 in accordance with the DTE supplied clock on pin 7.

If it is desired to have the Model 5500 supply clock for the equipment under test it is necessary to select the desired bit rate instead of EXTERNAL. In this case, the Model 5500 supplies timing to the DTE under test on pin 3 of the I/O connector. The Model 5500 analyzes the TD on pin 4 and TC on pin 3. RD on pin 1 and RC on pin 2 are generated by the Model 5500 internal clock source. A user supplied External clock signal into the User Clock BNC jack will cause the Model 5500 to generate data and clock at the externally applied clock rate when the Model 5500 is set to USER in the Bit Rate field.

Asynchronous DCE operation of the Model 5500 requires selection of the ASYNC mode, bit rate, character size, parity, and the number of stop bits. Data is generated and received in character format with no clock signals provided.

External DCE mode operation of the Model 5500 derives the signal from the ALT line on pin 13 of the DTE I/O connector. The state of this line will determine what mode the DTE is in and will set the Model 5500 (DCE) to the desired mode. User will set the desired functions correlating to this mode. Indications on this line will be on the "Bell 303 Format" menu and will be displayed "Mode [EXT - ASYNC]!
[SYNC]

3.2.1 Controls and Indicators

Front panel keys are available which enable the user to turn Data Set Ready (DSR) and Data Carrier Detect (DCD) "ON" and "OFF" in DCE mode of operation. In addition, these conditions, and any other settings can also be controlled from a remote terminal using the RS-232 or IEEE-488 rear panel remote control ports.

The twelve green LED indicators provide status of the primary interface signals leads as discussed earlier in section 3.1.1.

Remote Port Additions

CPMODE [Self Test]
[Remote]

MD [ASYNC]
[SYNC]
[EXT]